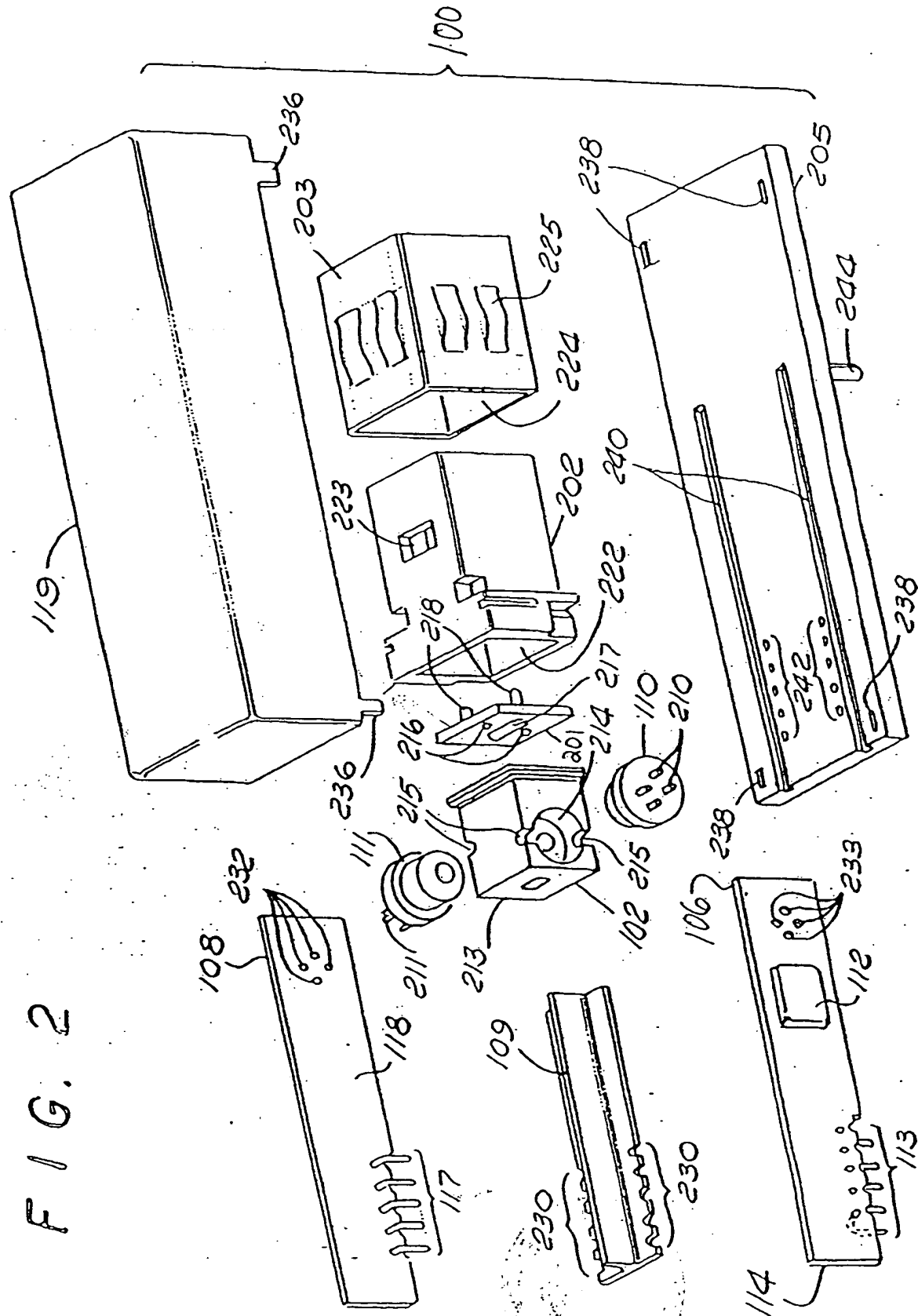
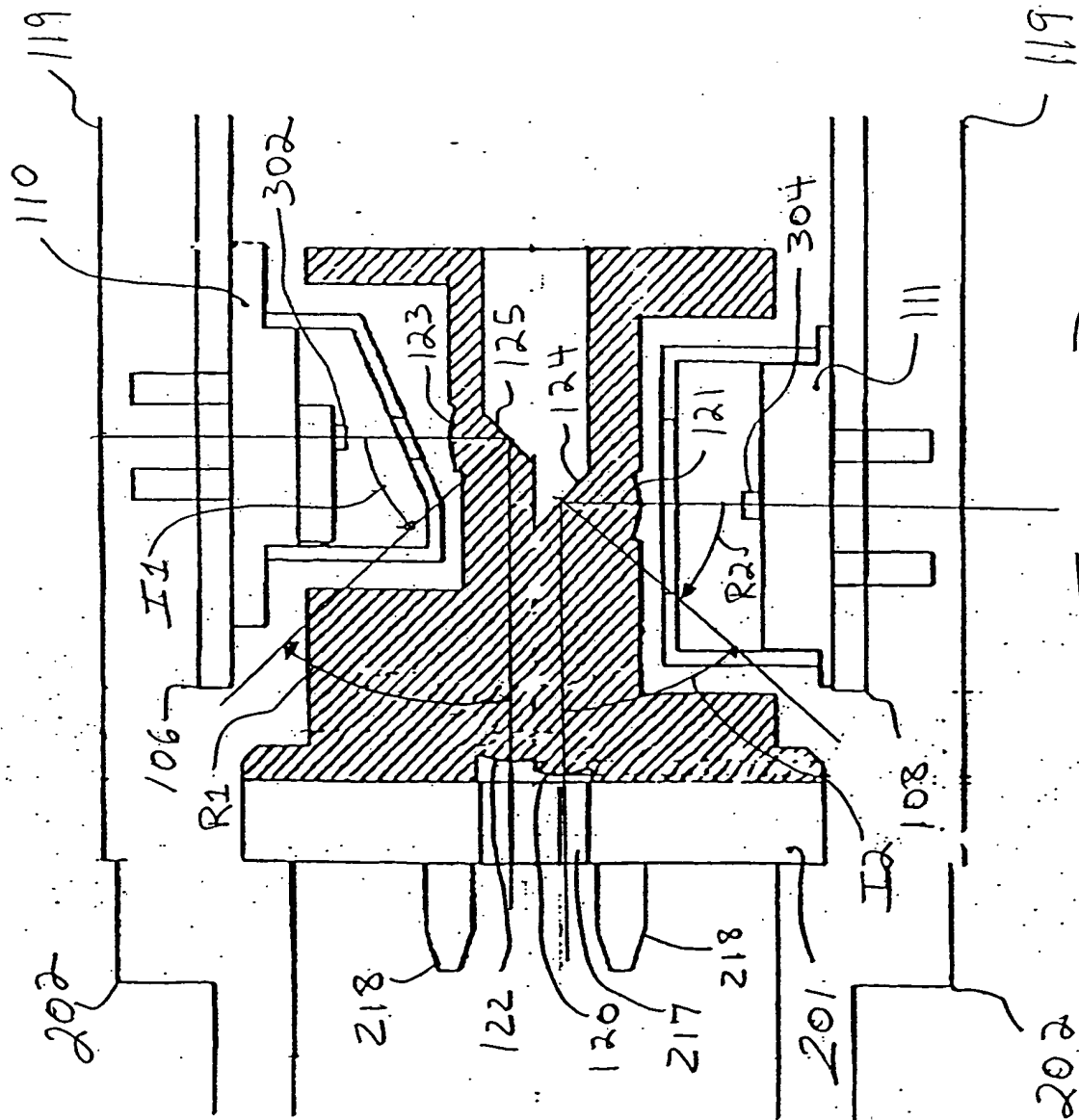




FIG. 2



[illegible]

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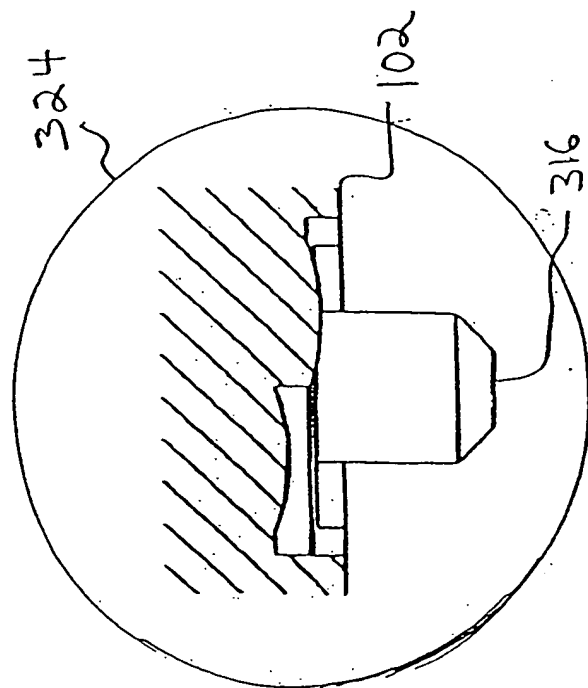


FIG. 3B

FIG. 3C

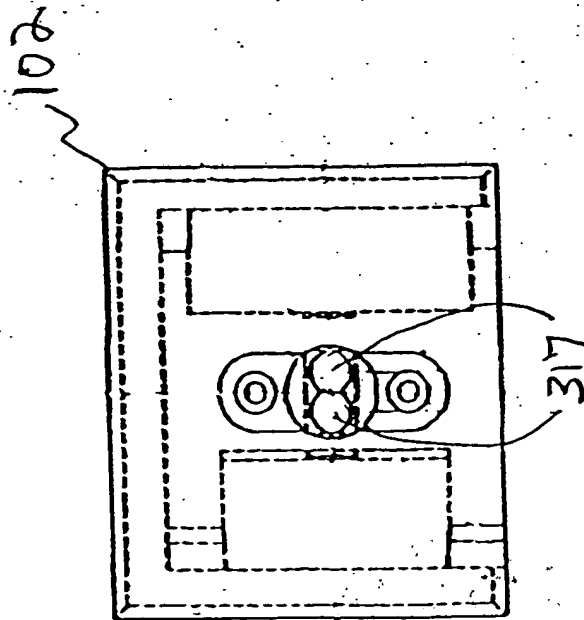


FIG. 3C

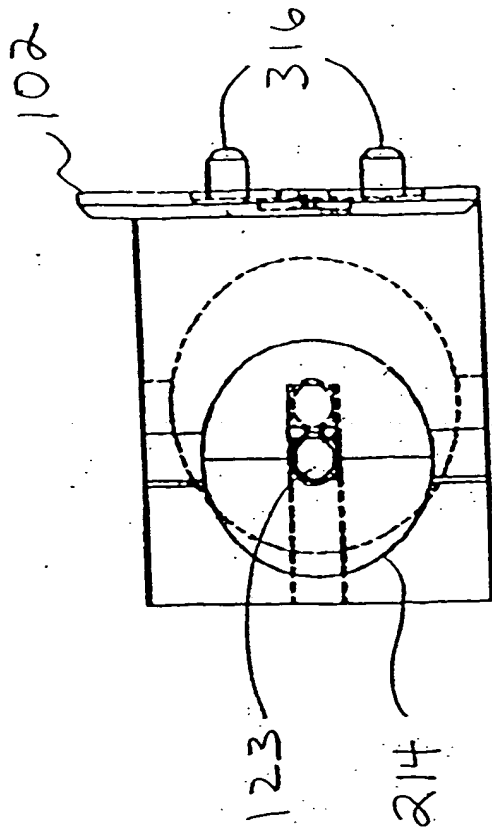


FIG. 3F

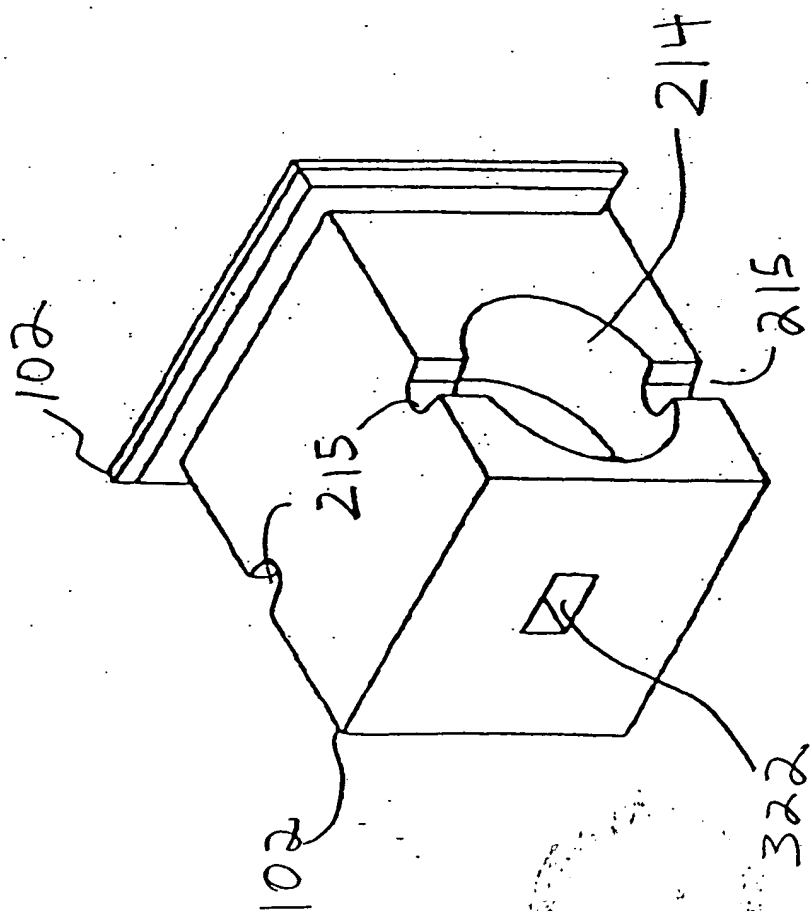


FIG. 3D

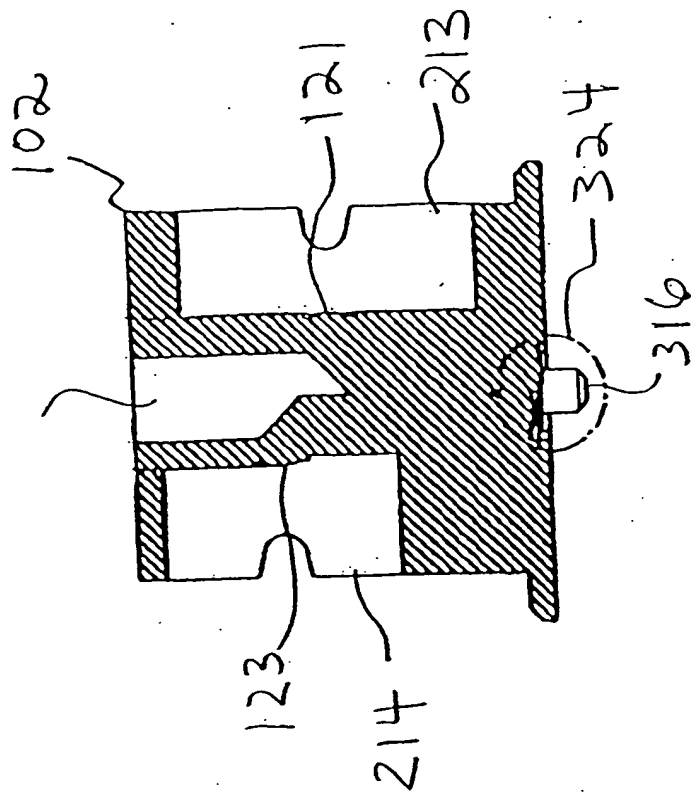


FIG. 3H

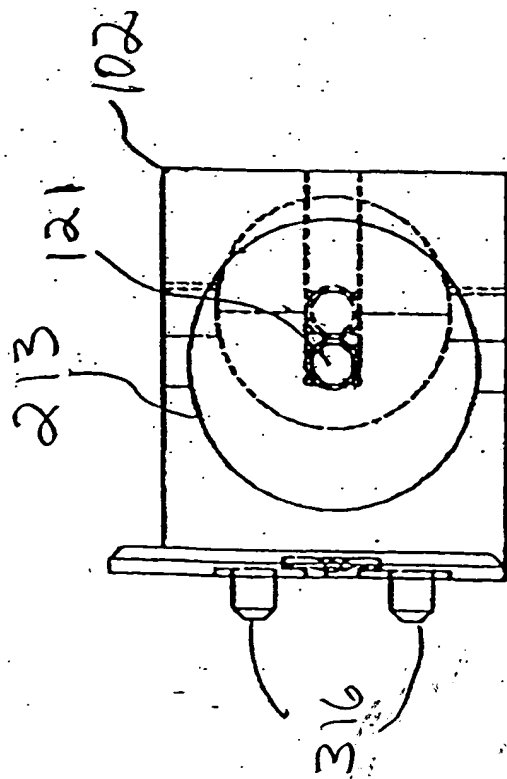


FIG. 36

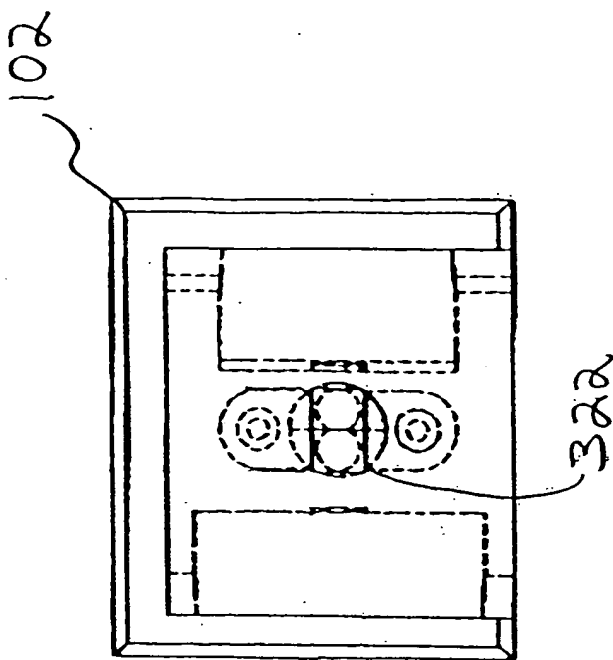


FIG. 3E

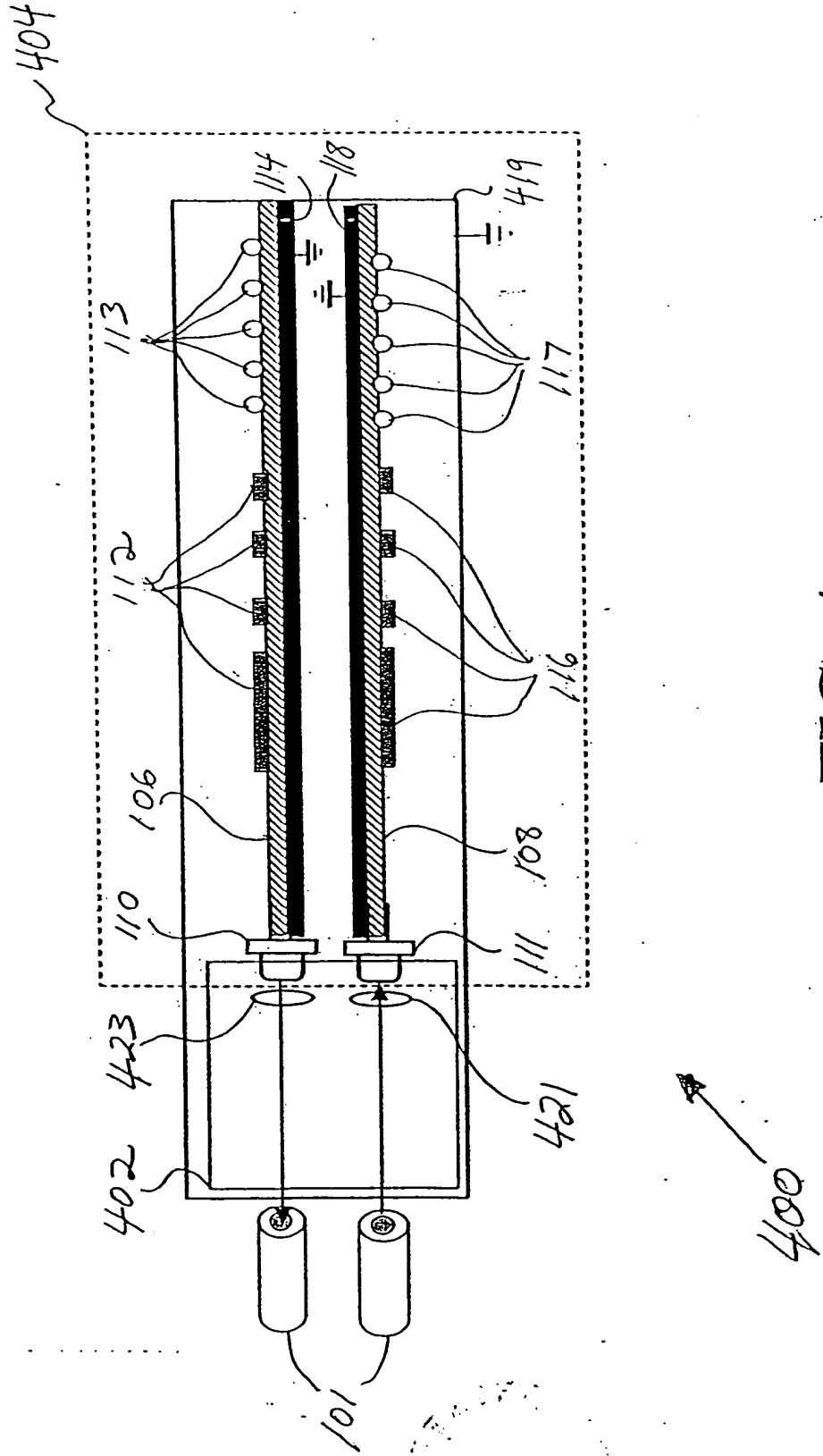


FIG. 4

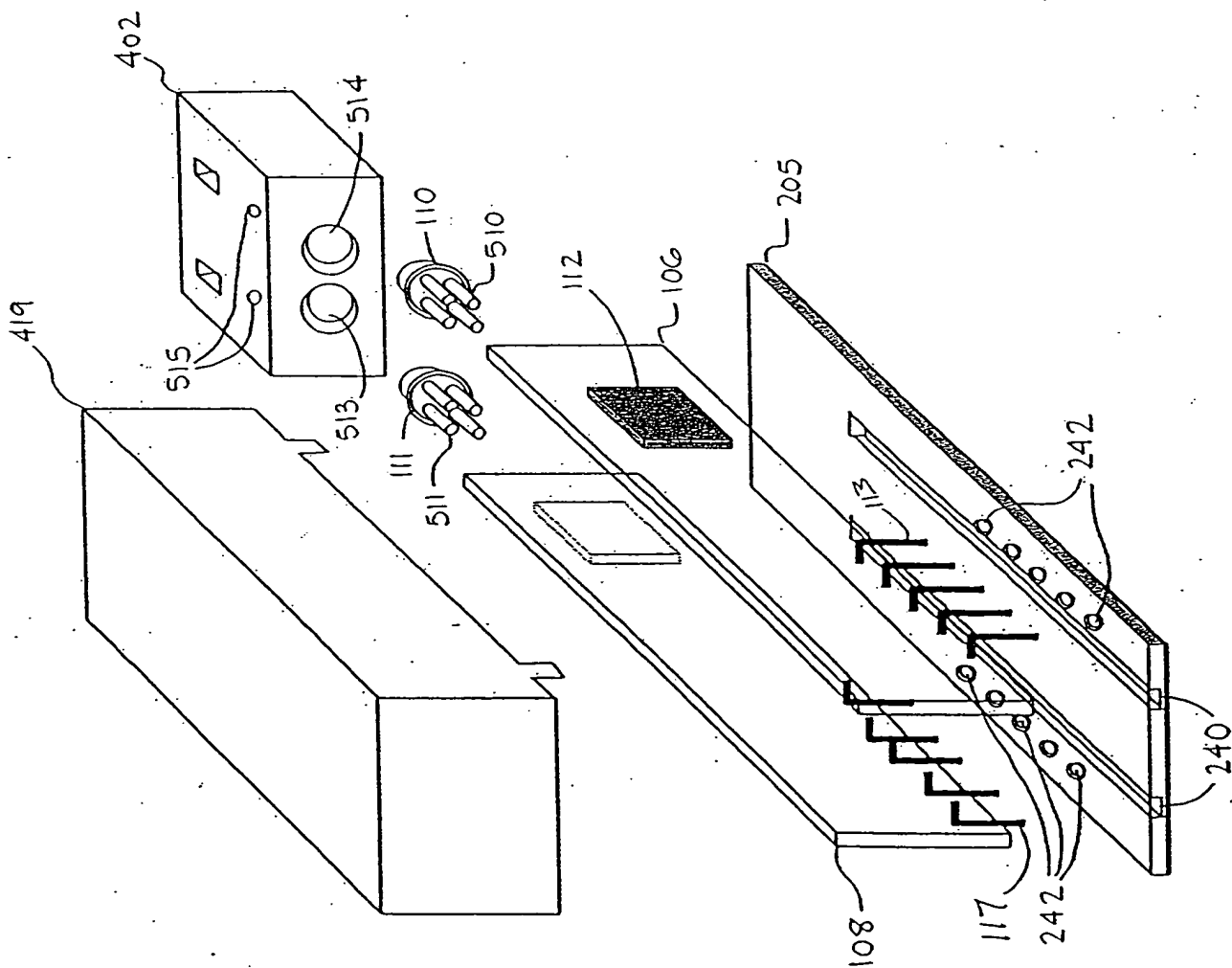


FIG. 5A

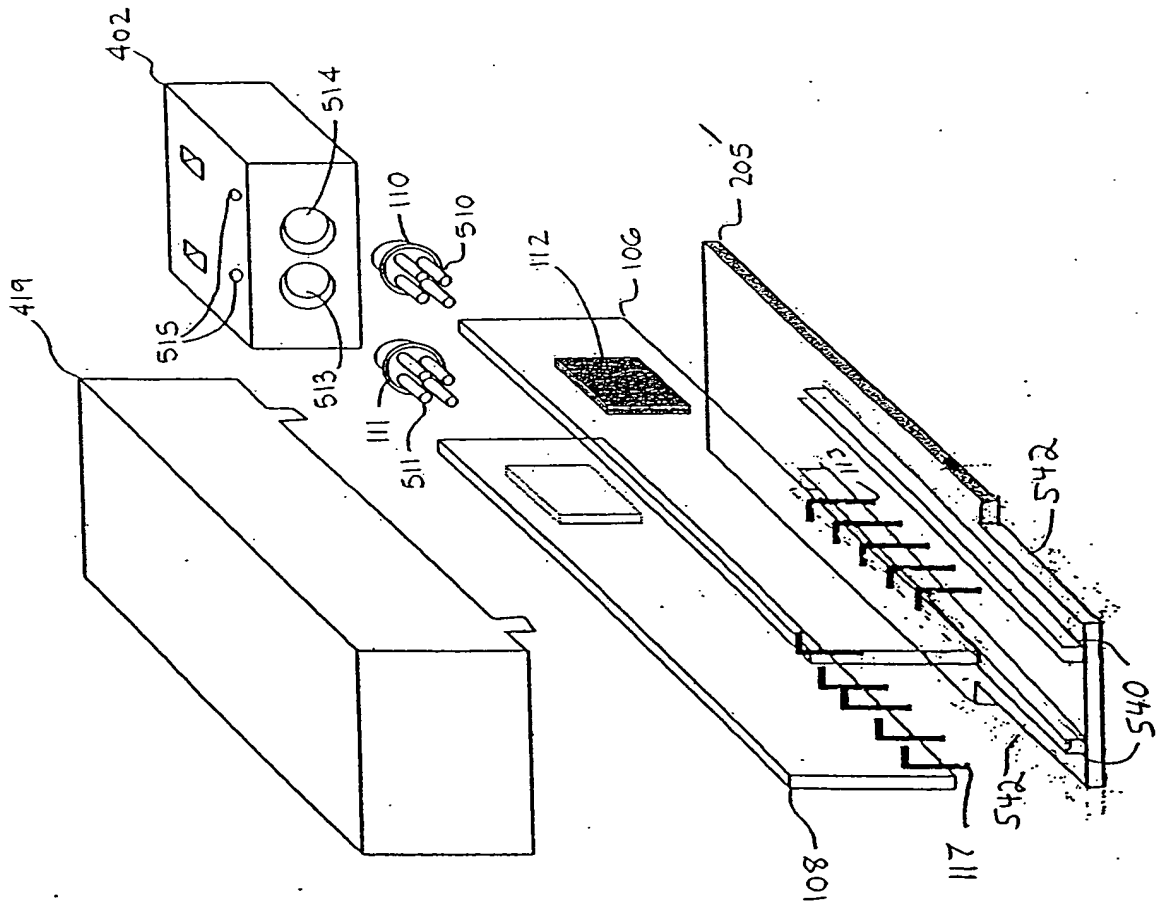


FIG. 5B

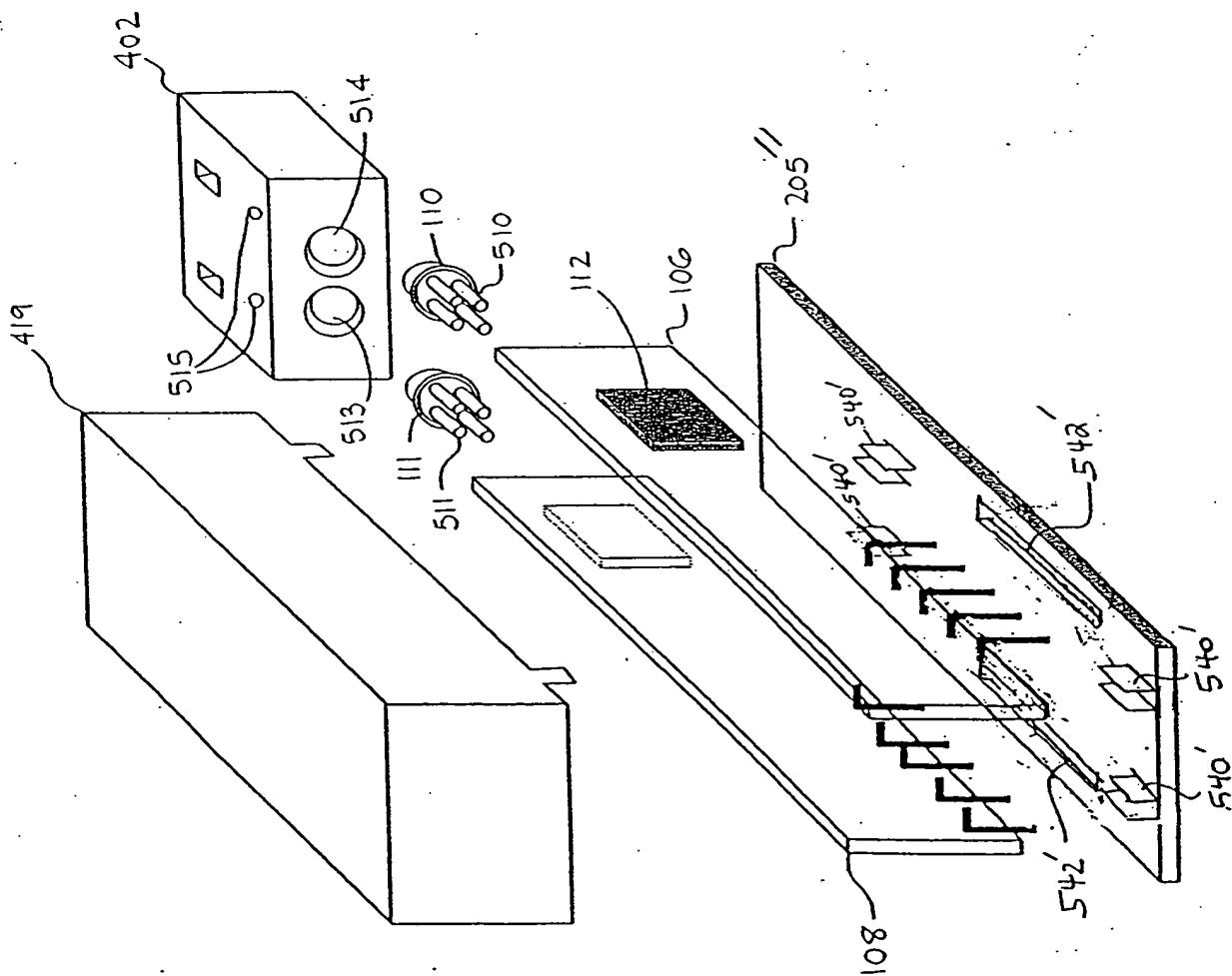


FIG. 5C





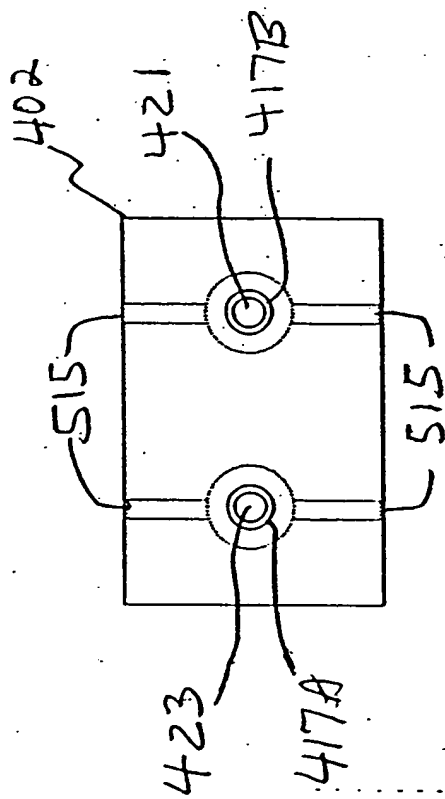


FIG. 6B

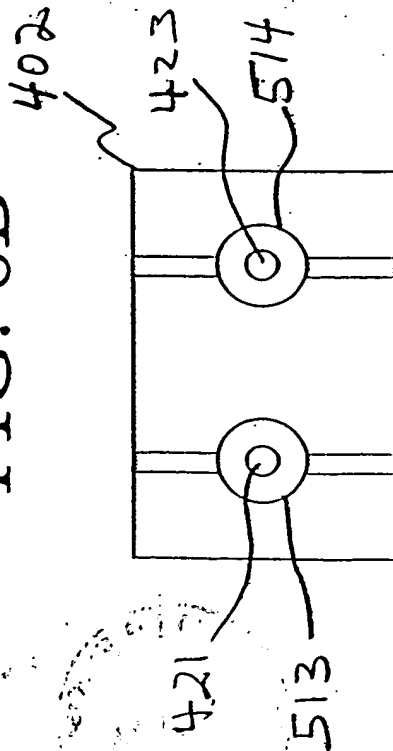


FIG. 6C

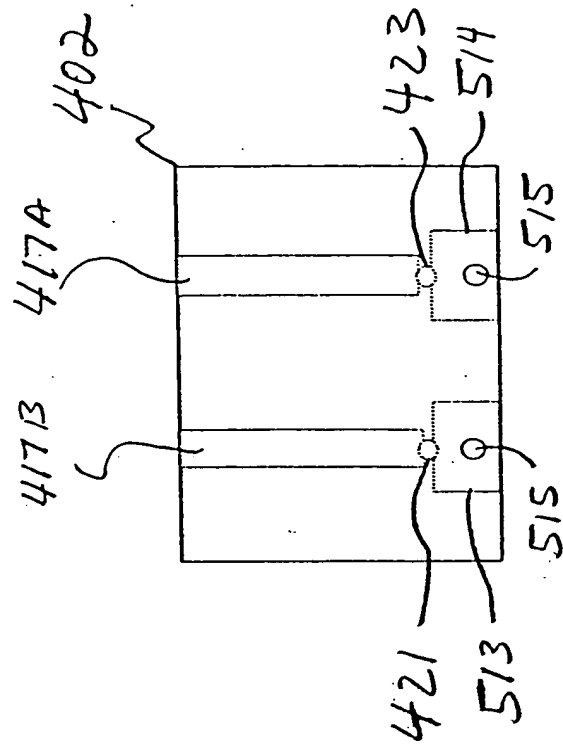


FIG. 6D

FIG. 7A

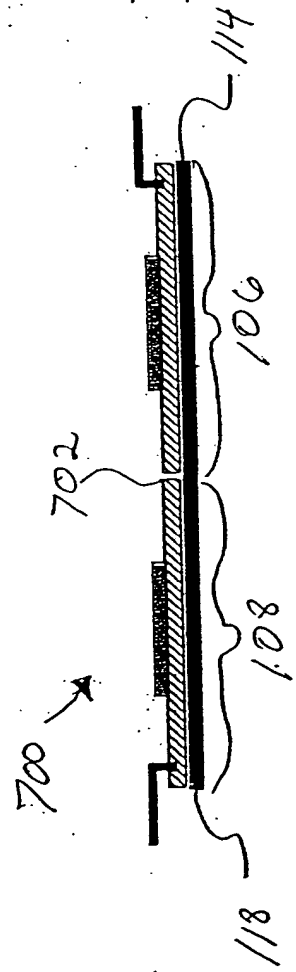


FIG. 7A

FIG. 7B

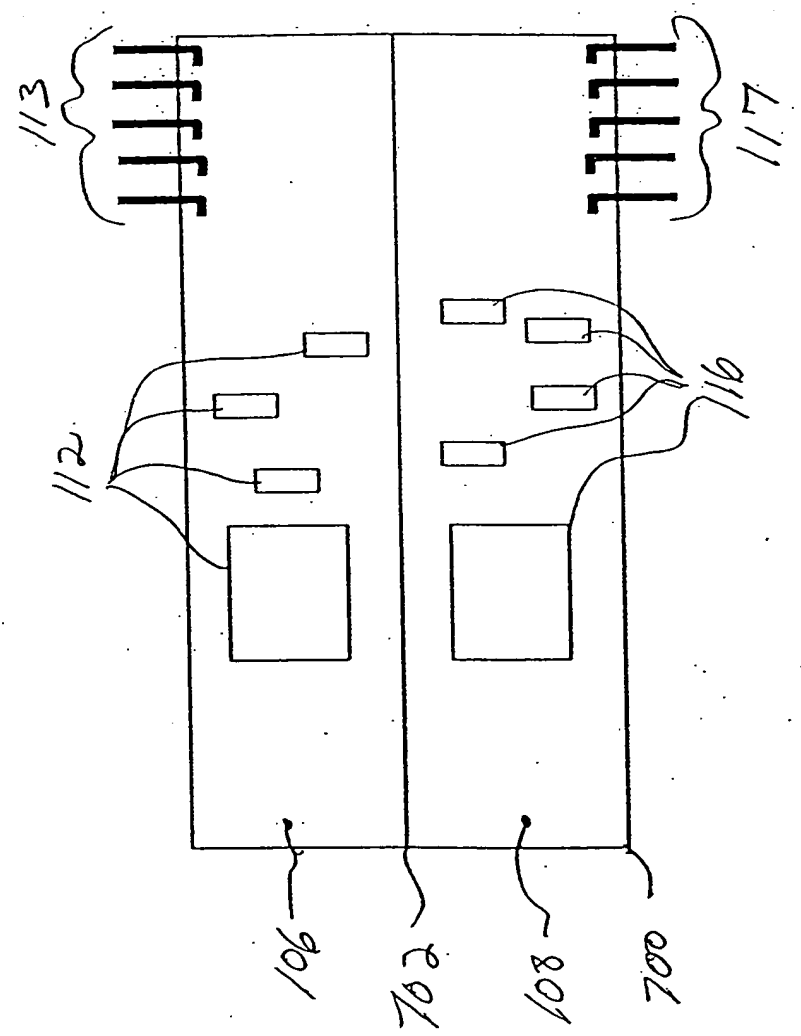


FIG. 10

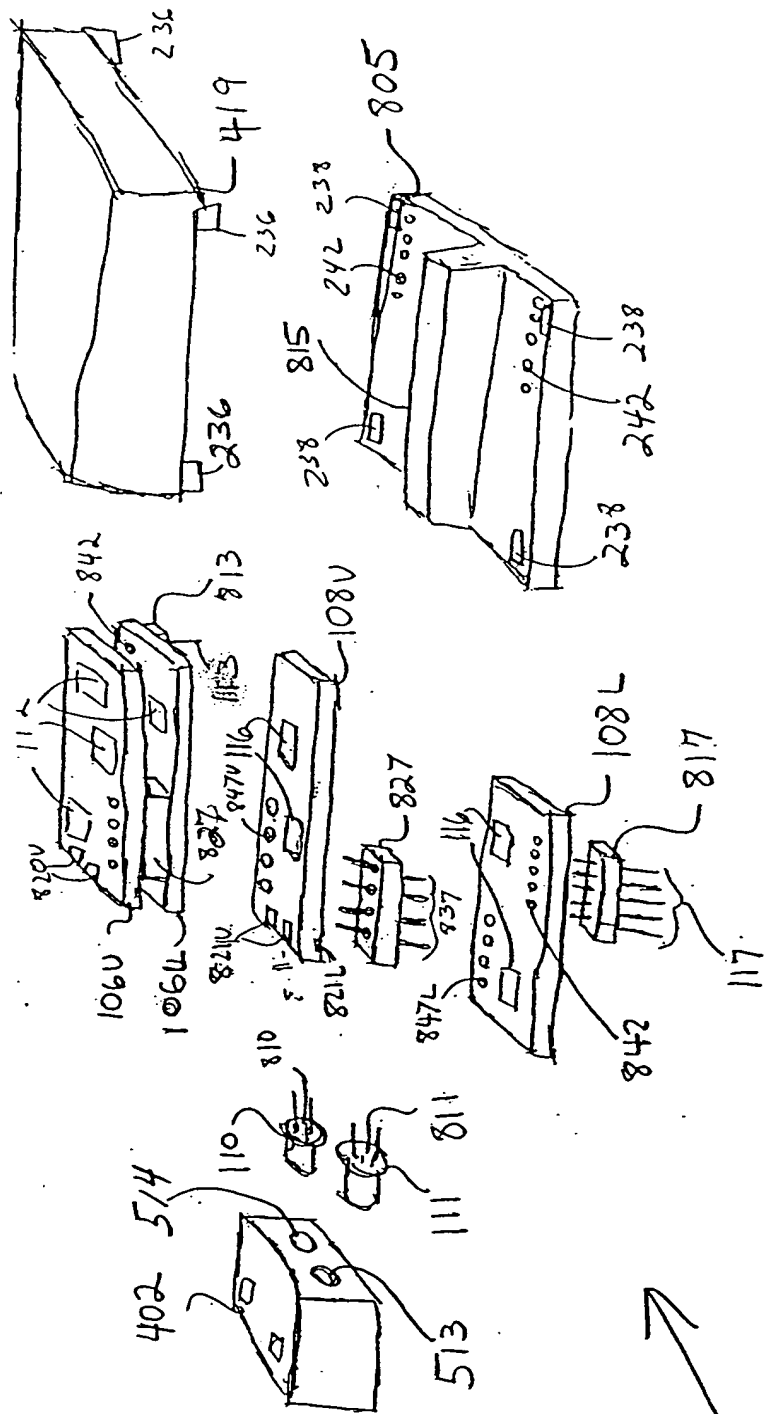


FIG. 8A

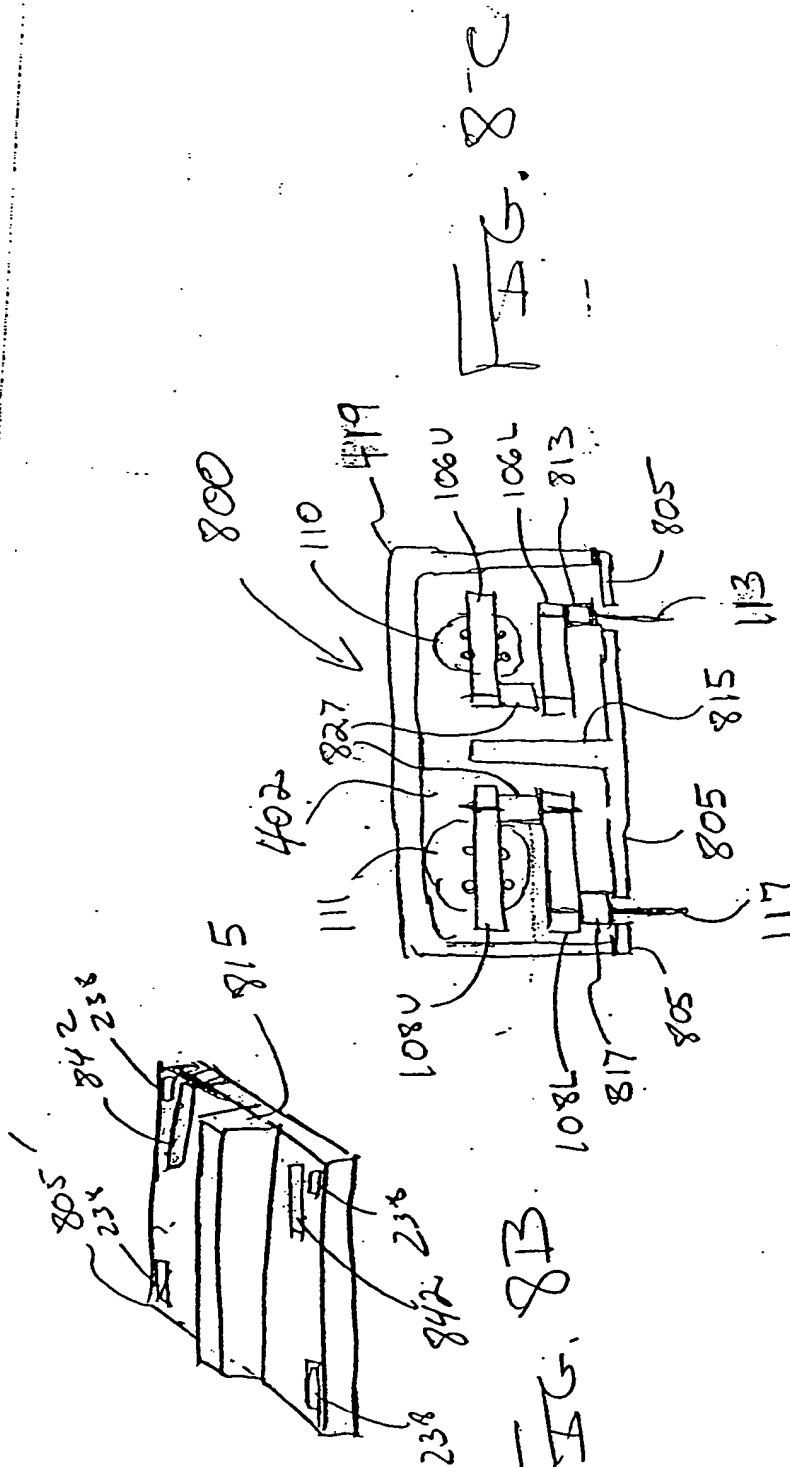
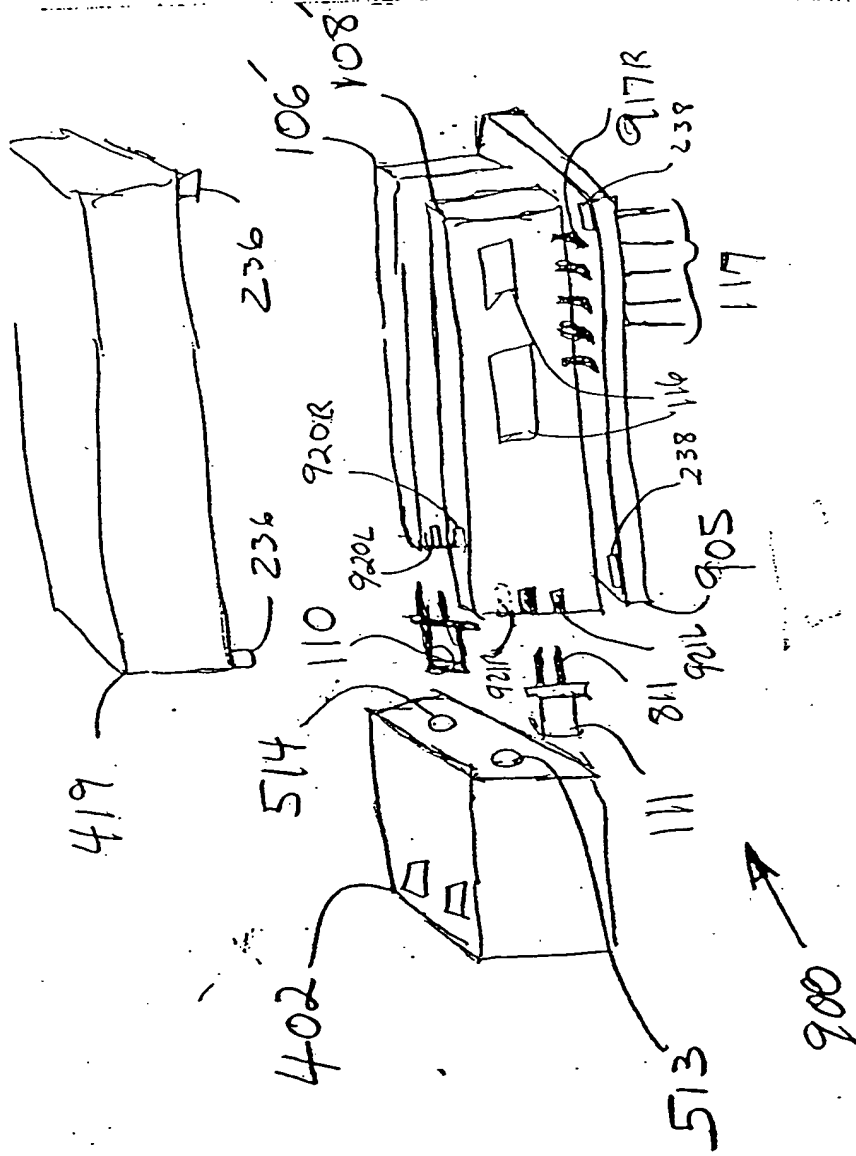
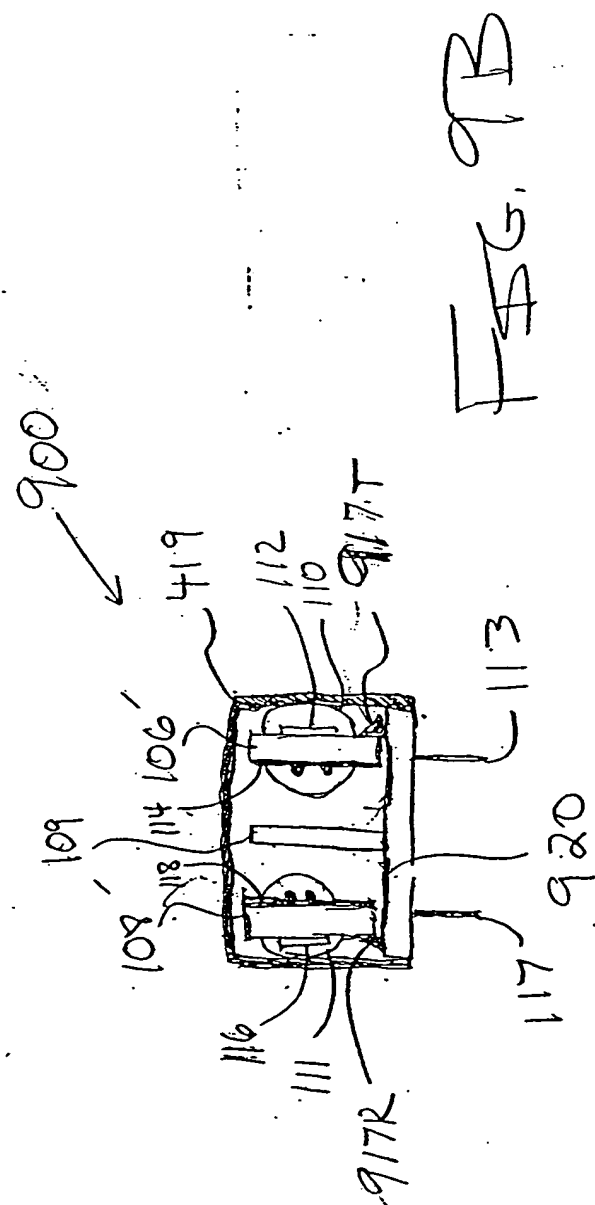
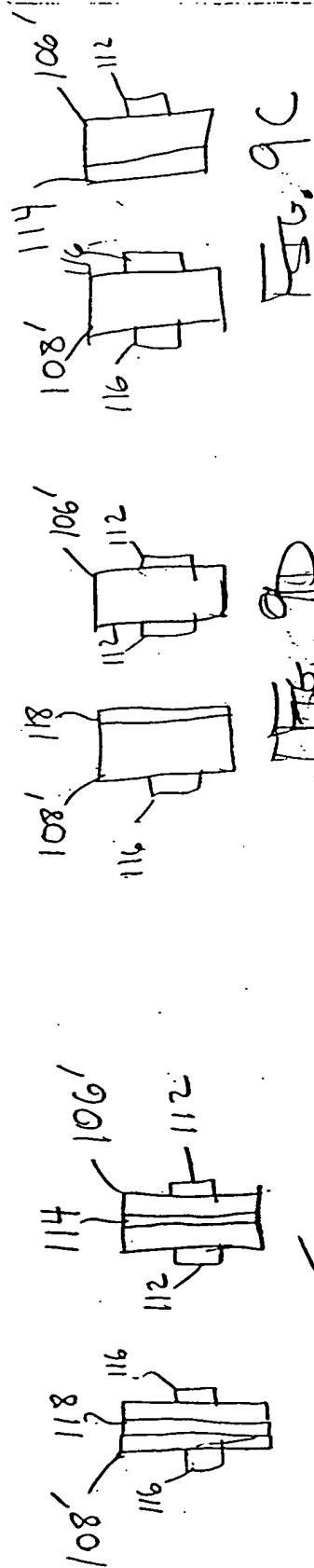
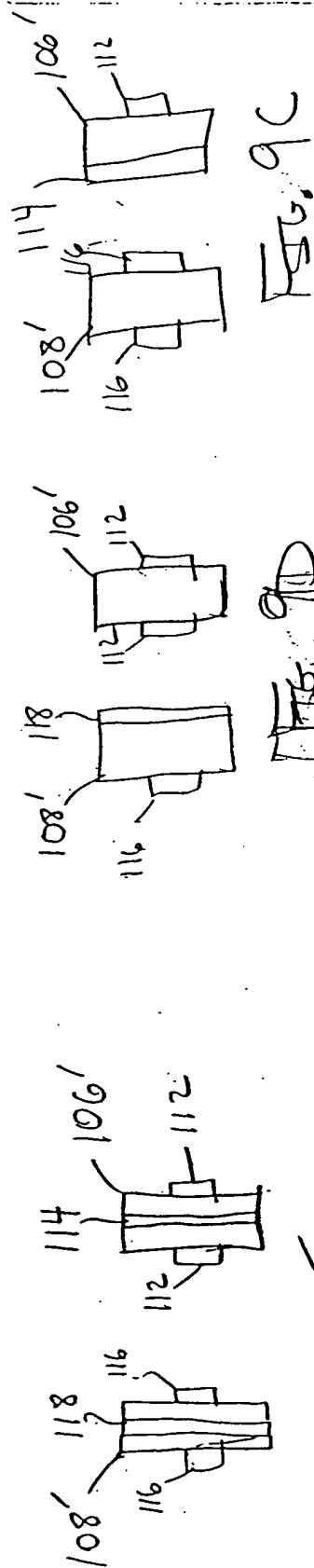
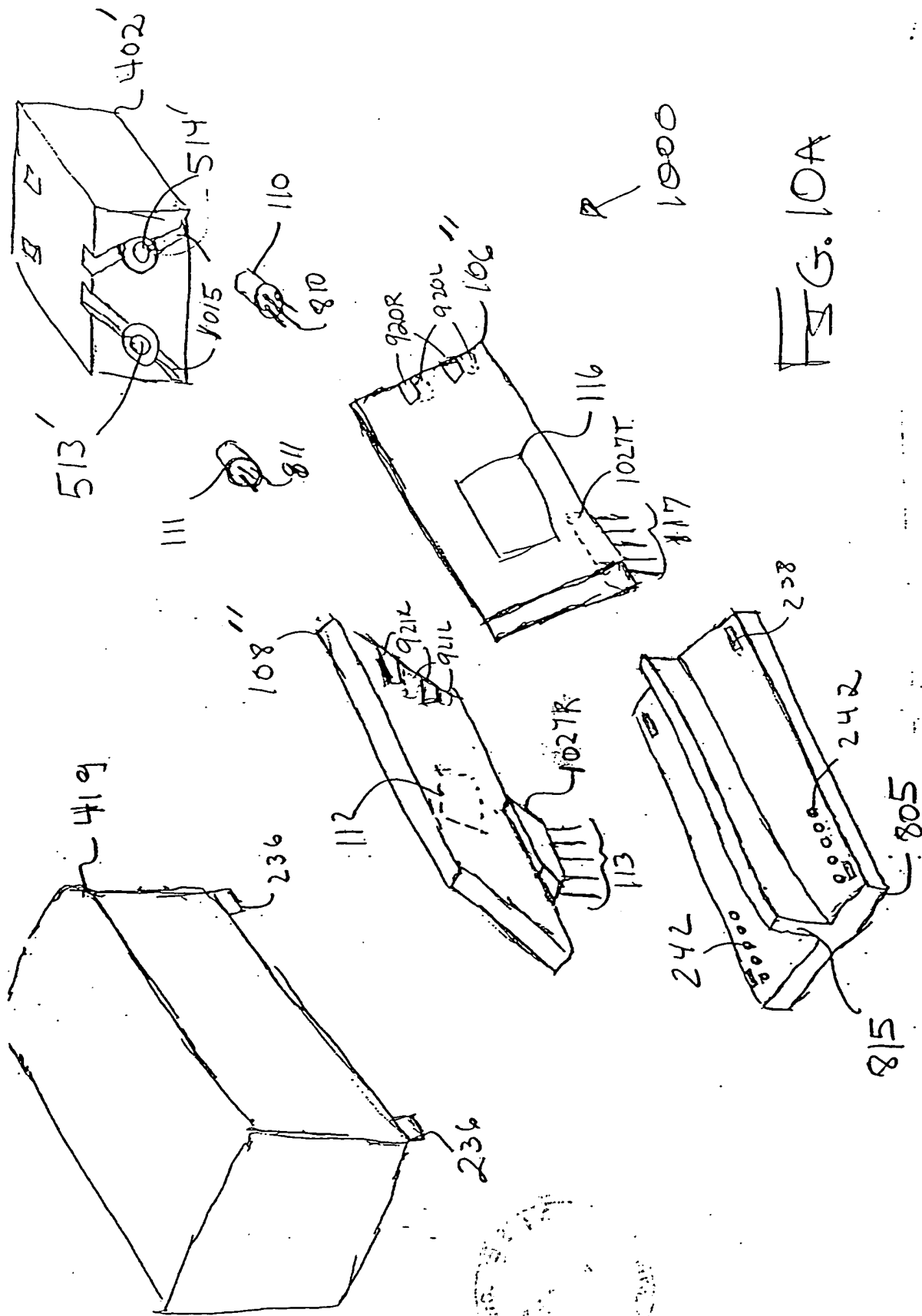


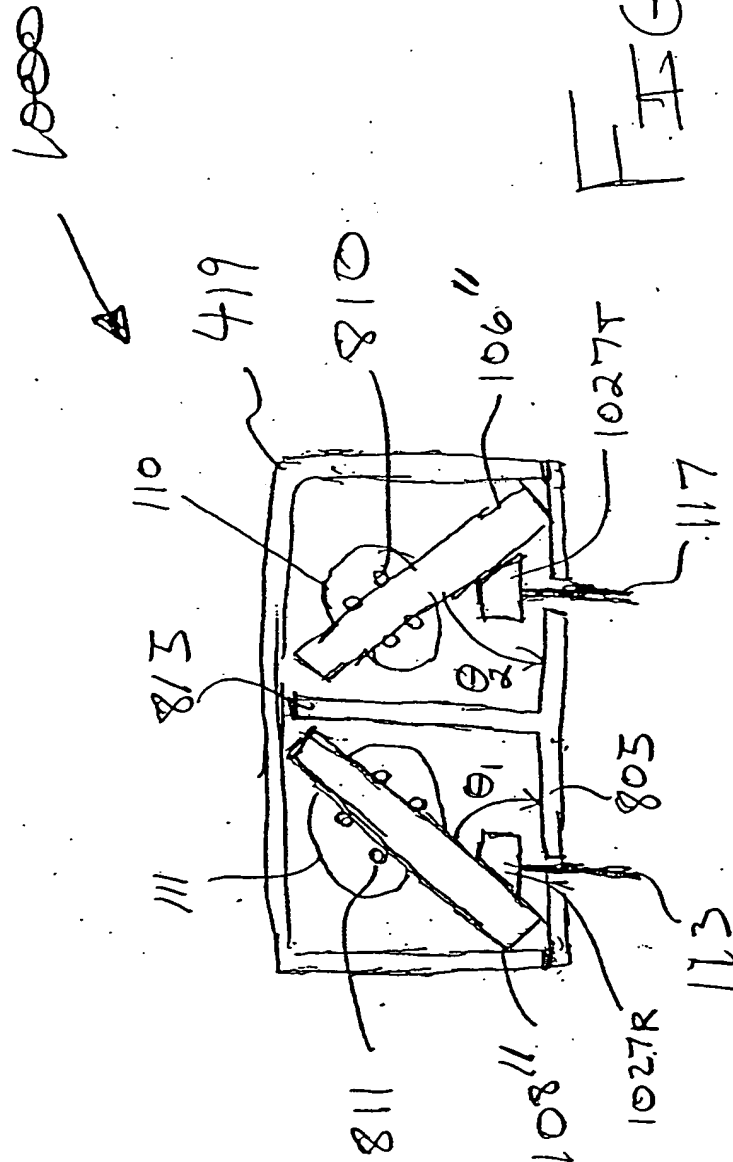
FIG. 9A



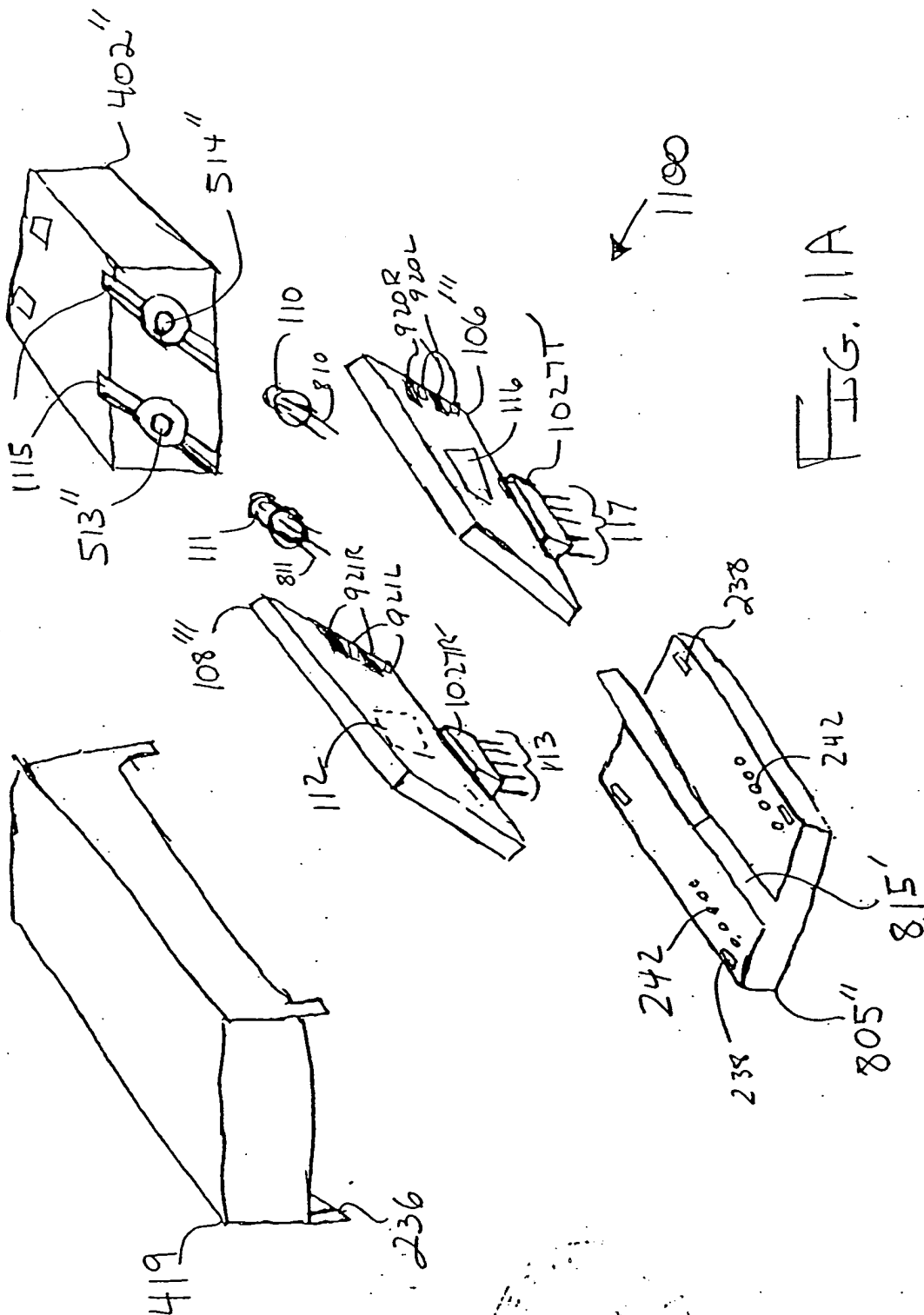
[illegible]



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10. MO WH 6



1100

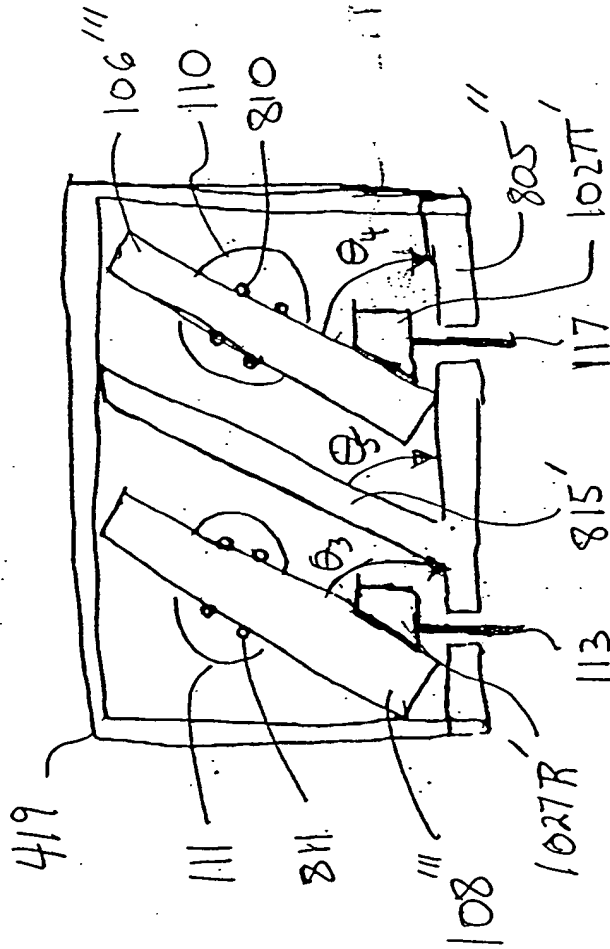
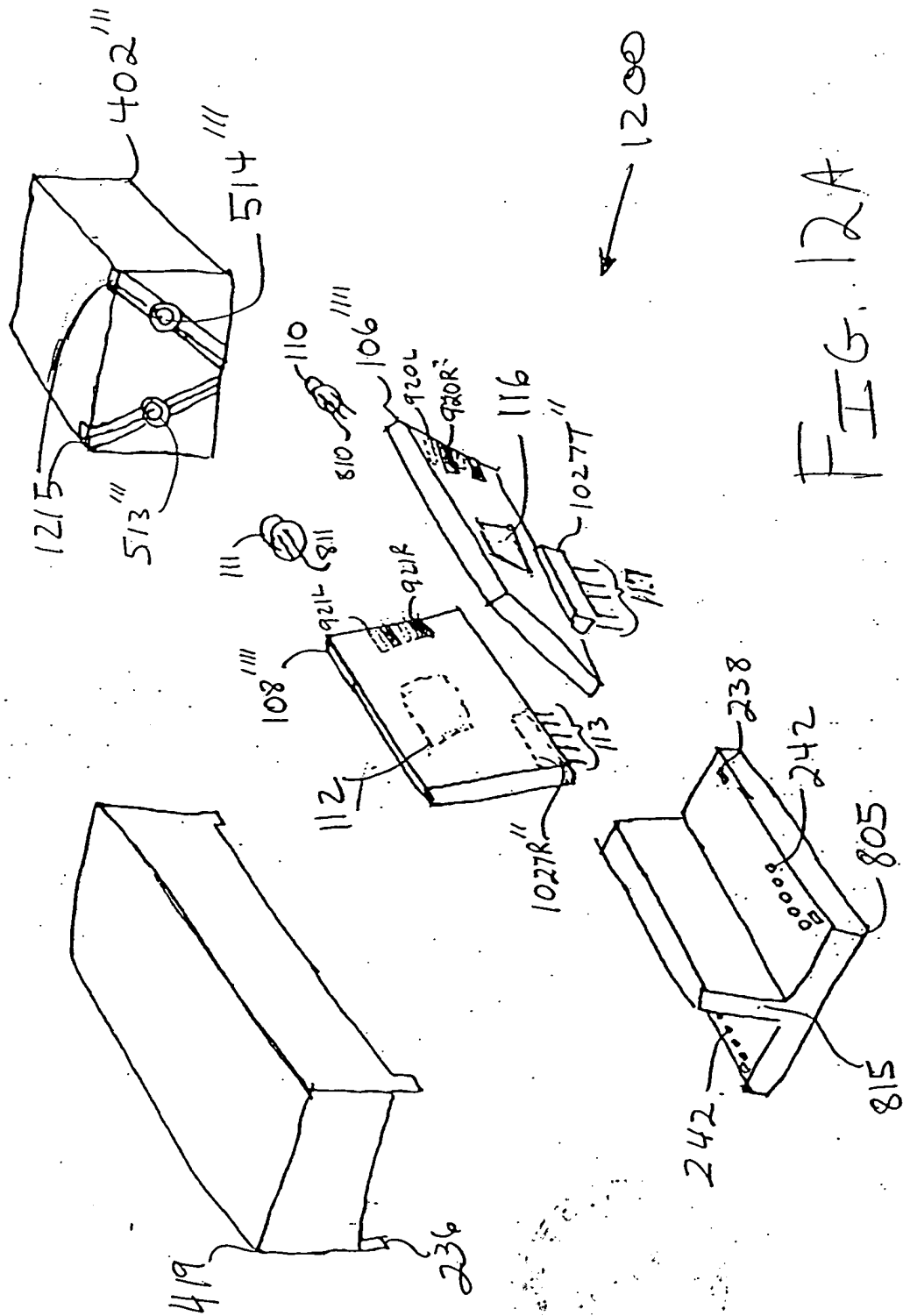


FIG. 11B



1200

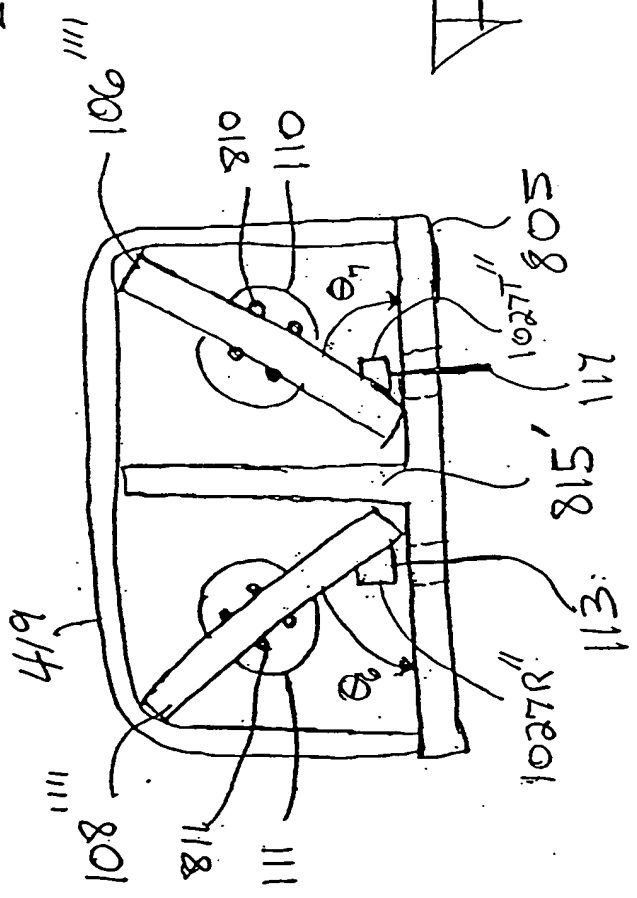


FIG. 12B

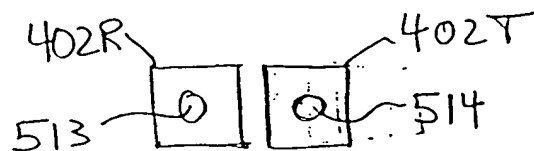


FIG. 13

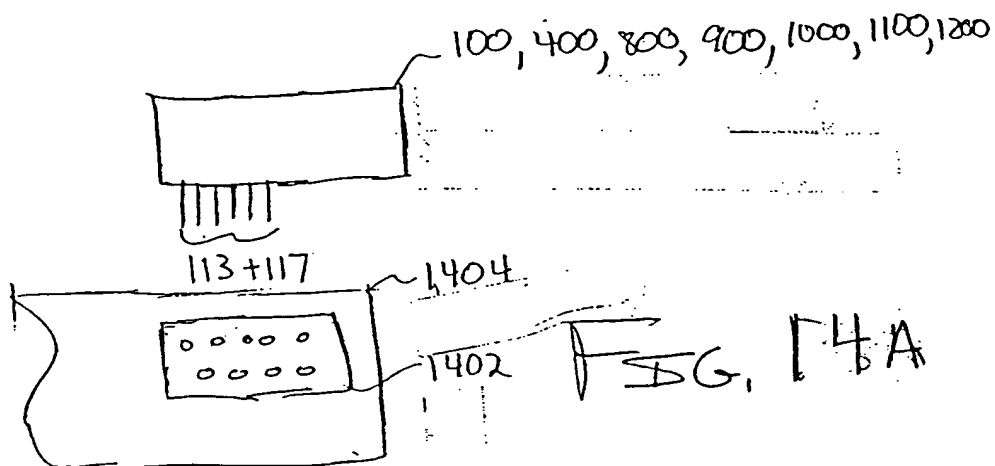


FIG. 14A

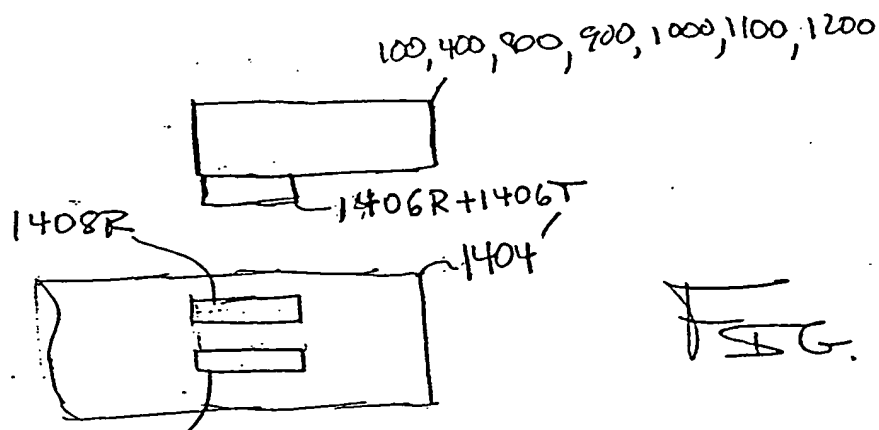


FIG. 14B

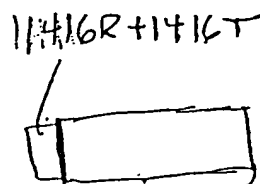
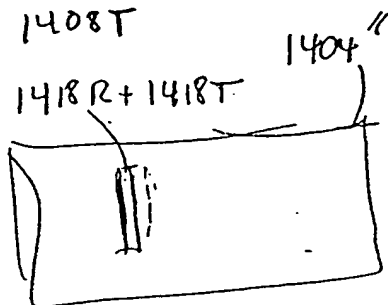
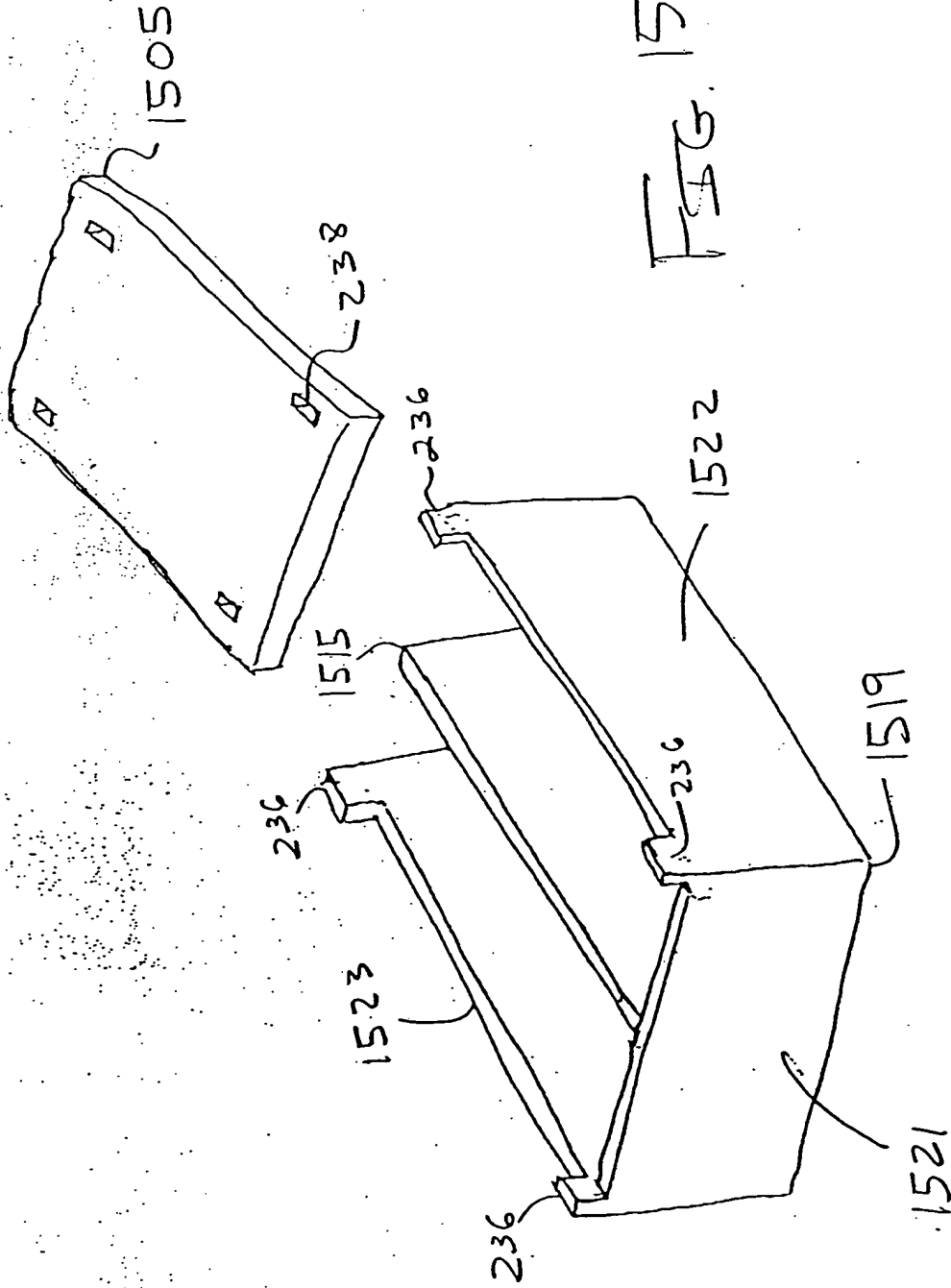


Fig. 14C

100, 400, 800, 900, 1000, 1100, 1200

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1000

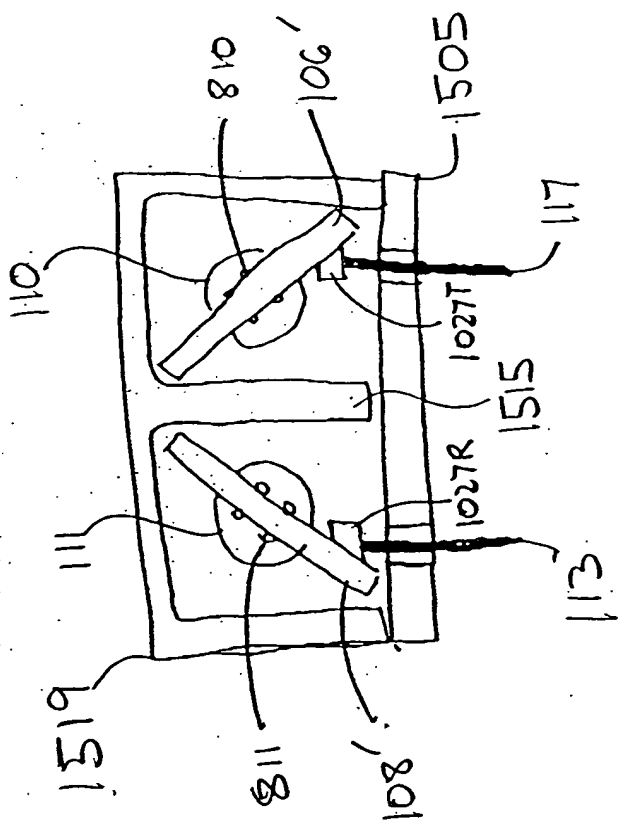


FIG. 15B

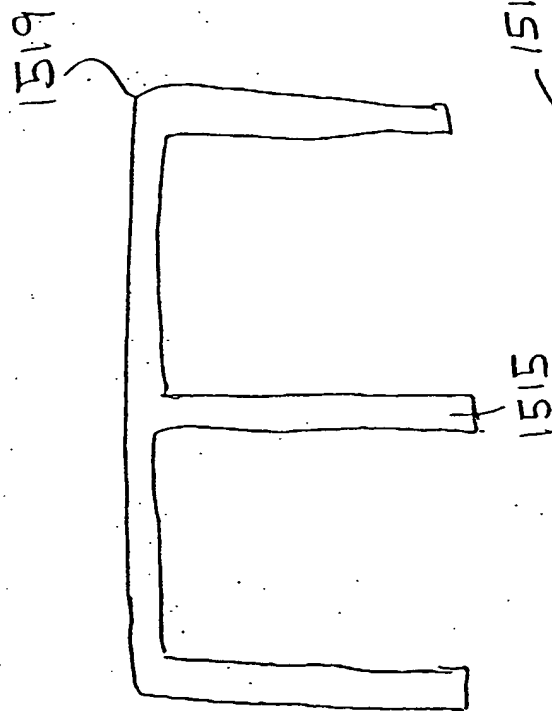


FIG. 15C

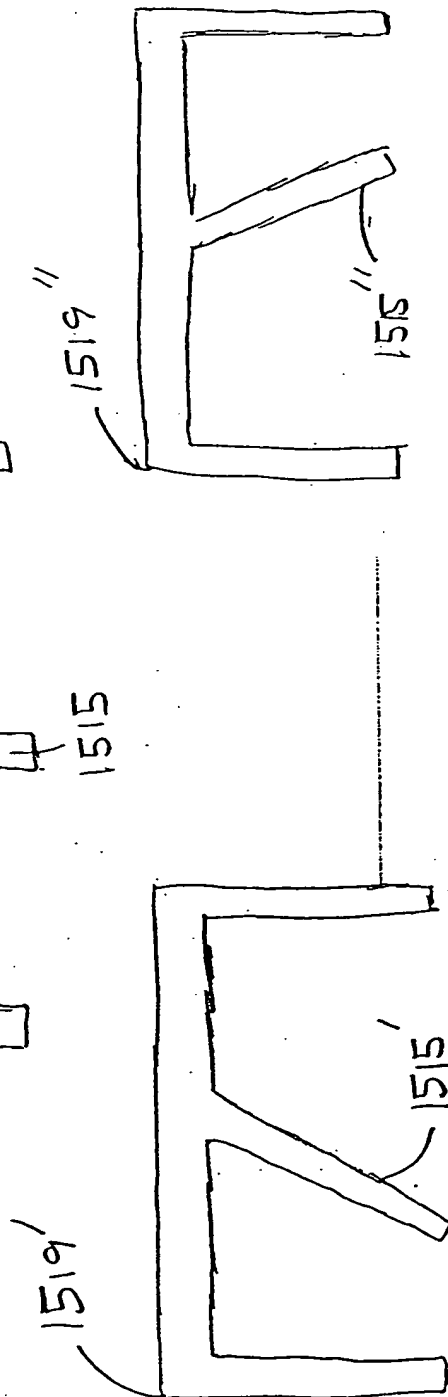


FIG. 15D

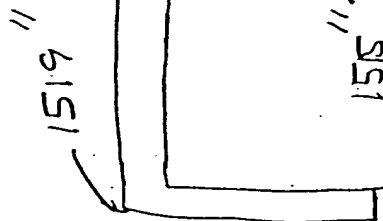


FIG. 15E

FIG. 15

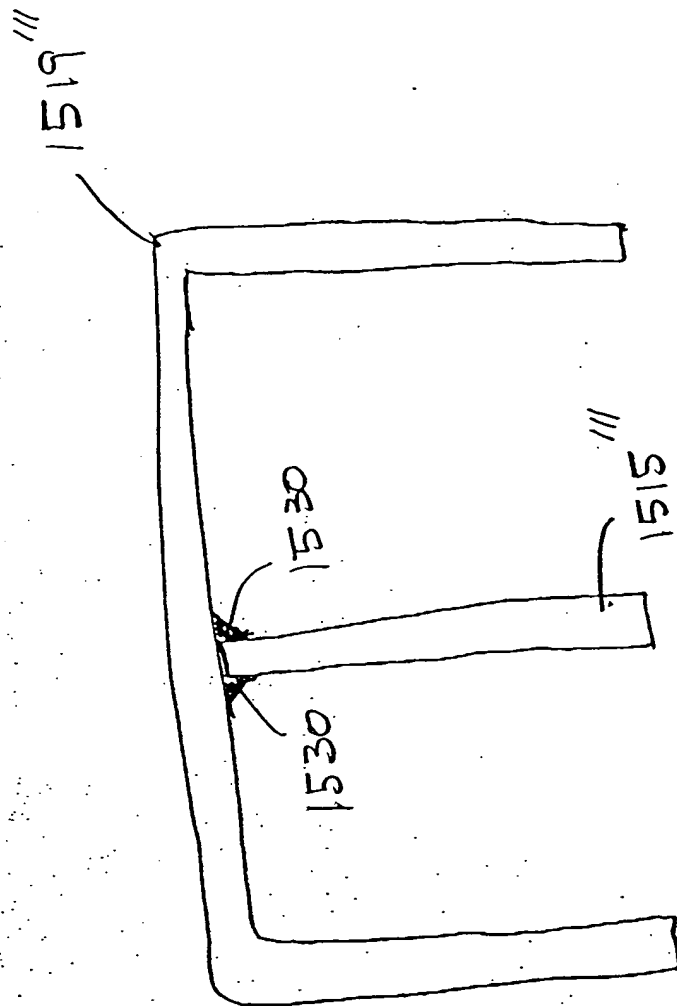


FIG. 15

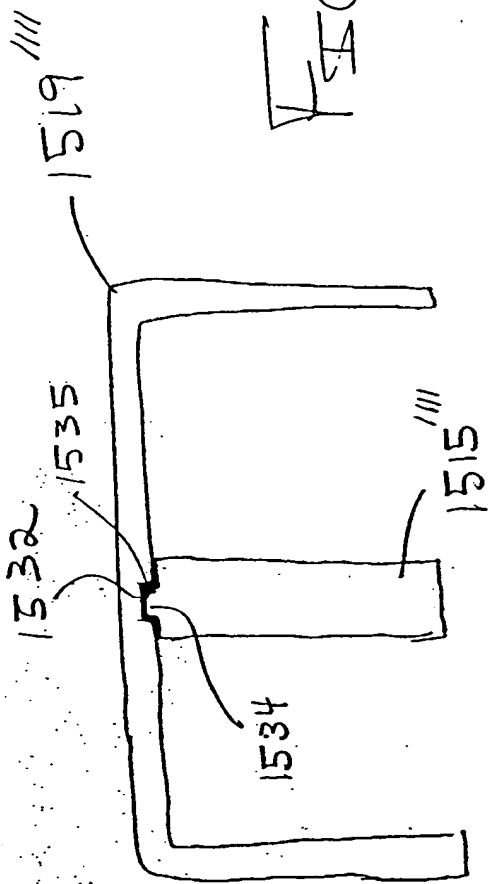


FIG. 15G

1600

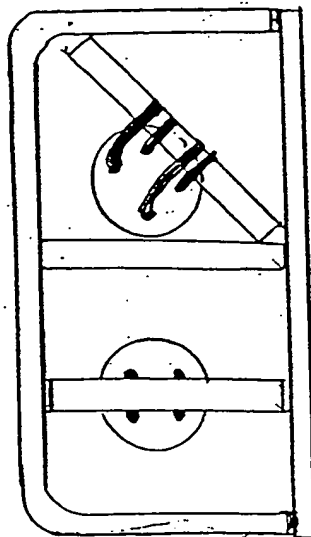


FIG. 16A

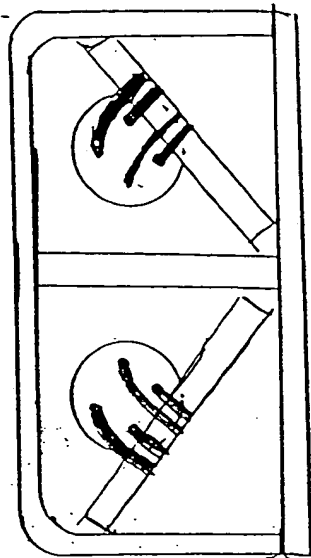


FIG. 16B

1602

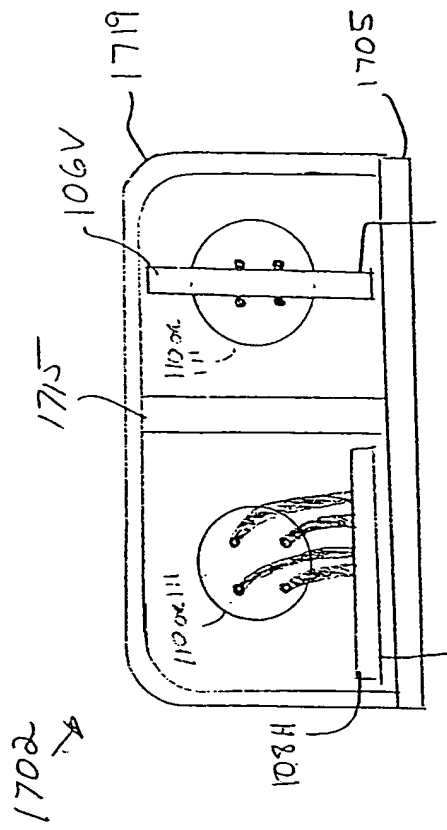


FIG. 17A

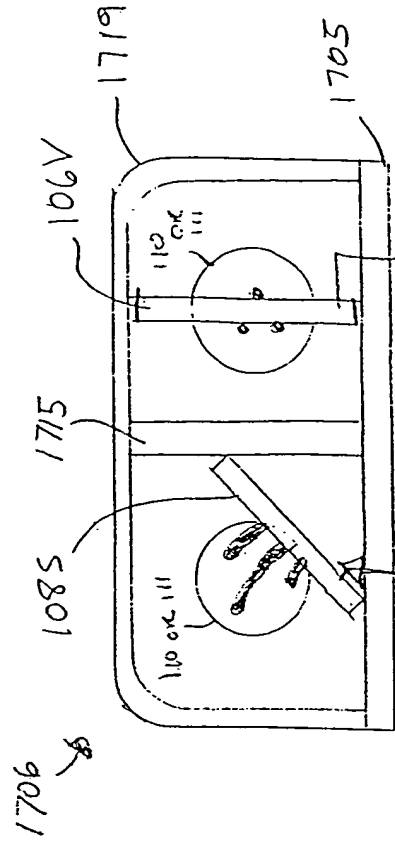


FIG. 17B

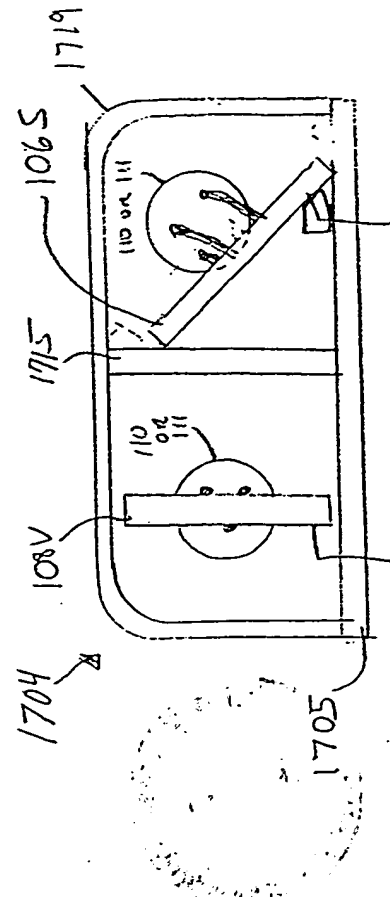


FIG. 17C

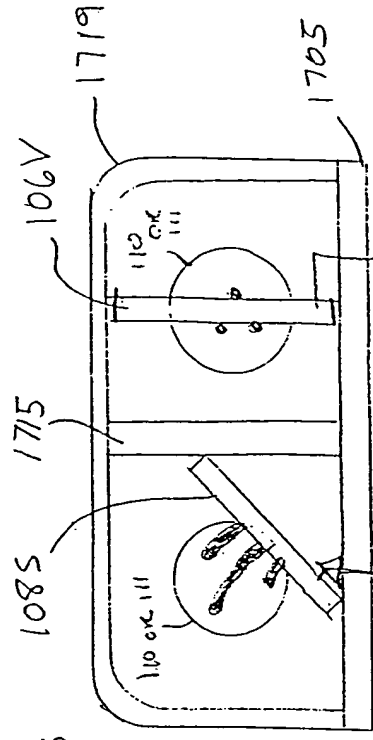


FIG. 17D

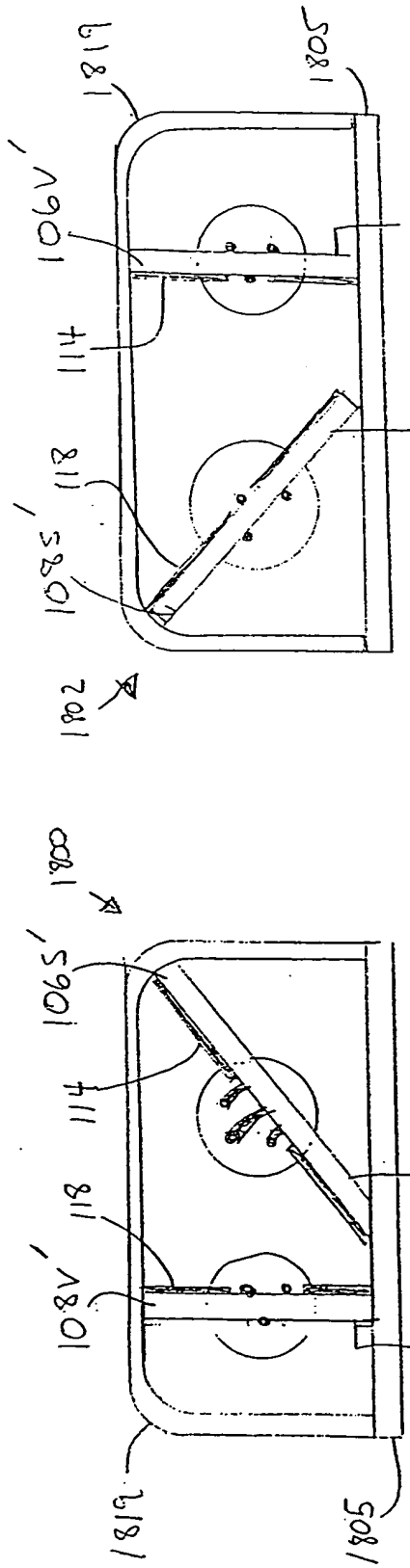


FIG. 18A

FIG. 18B

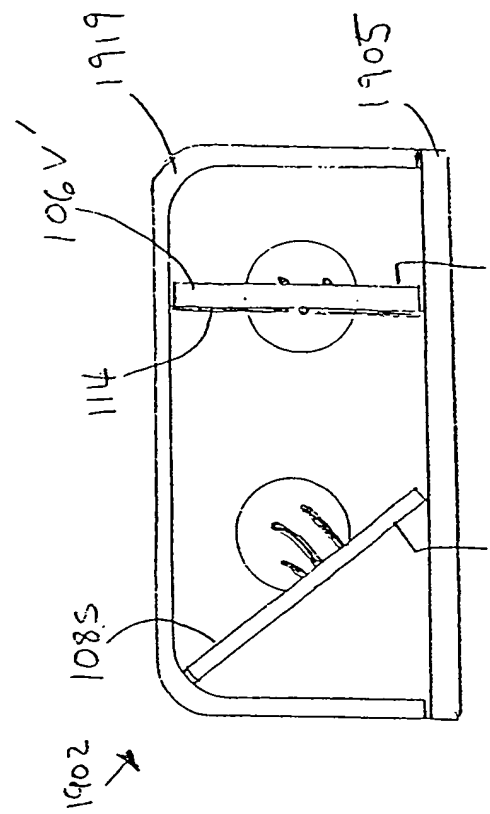


FIG. 18B

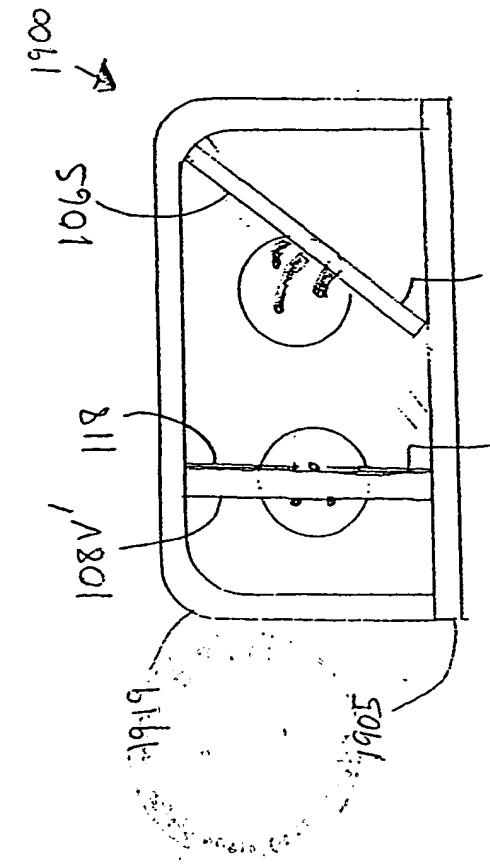


FIG. 19A

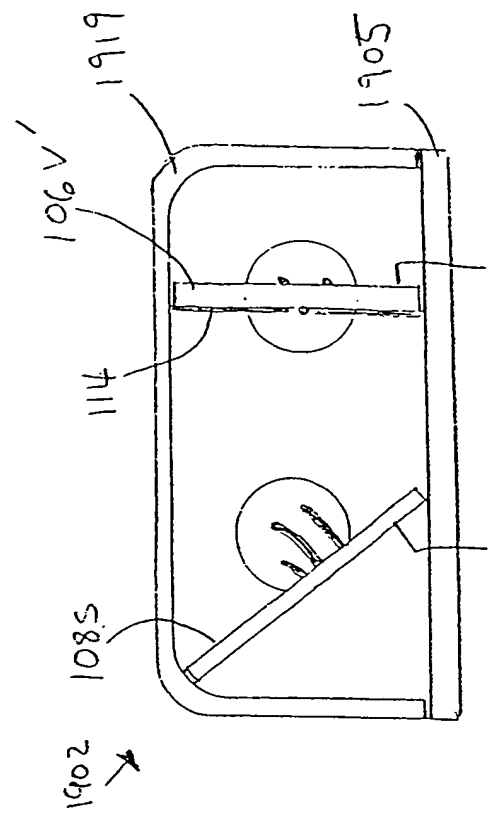


FIG. 19B

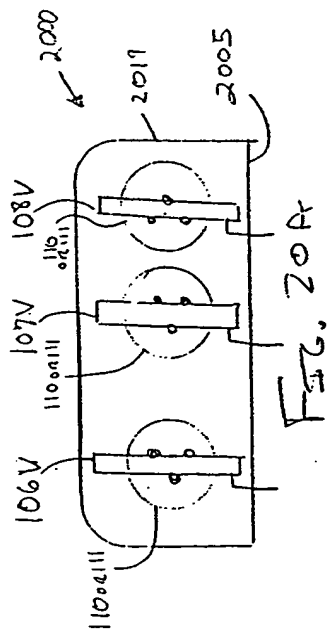


FIG. 20A

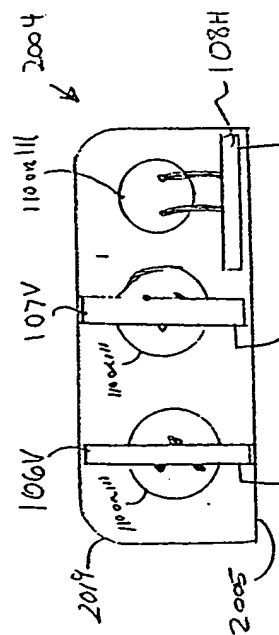


FIG. 20C

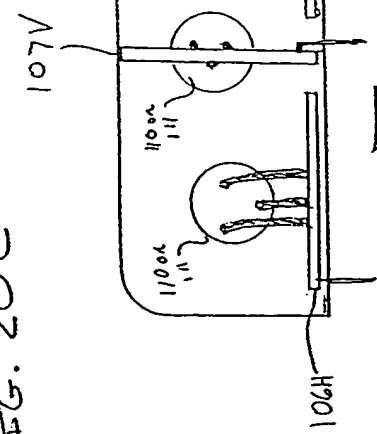


FIG. 20E

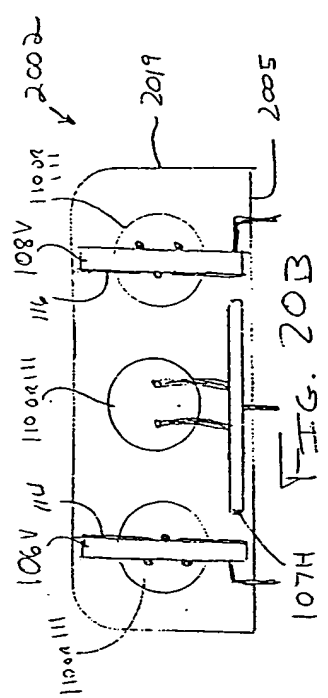


FIG. 20B

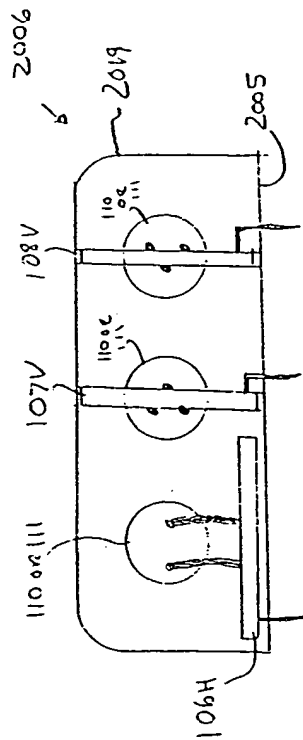


FIG. 20D

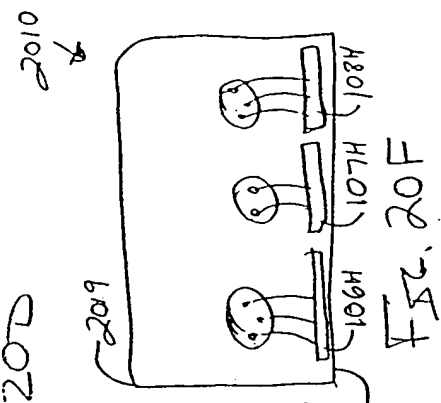
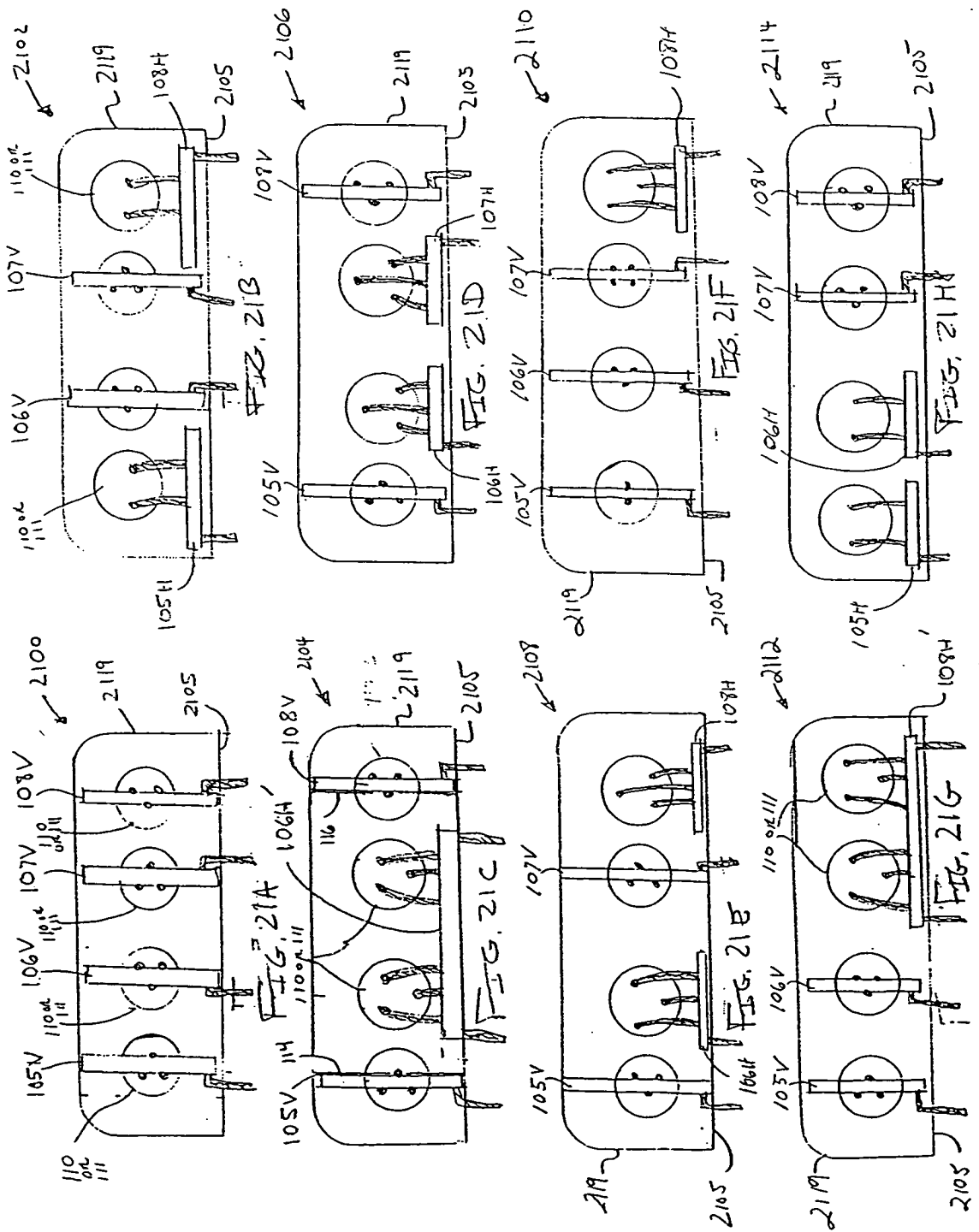


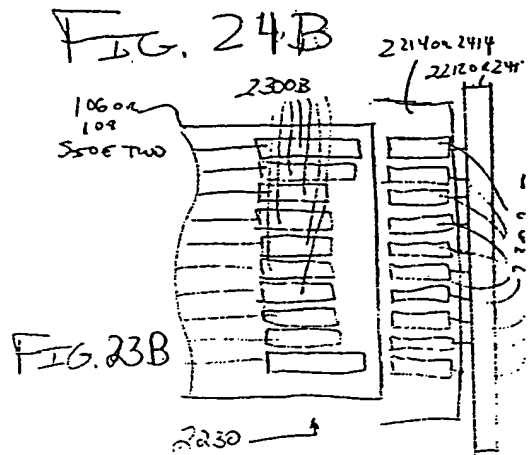
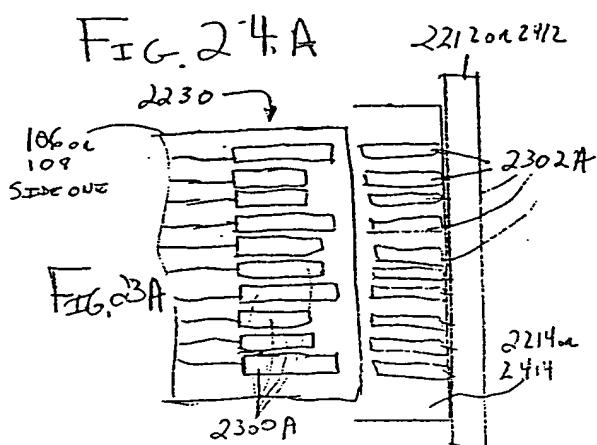
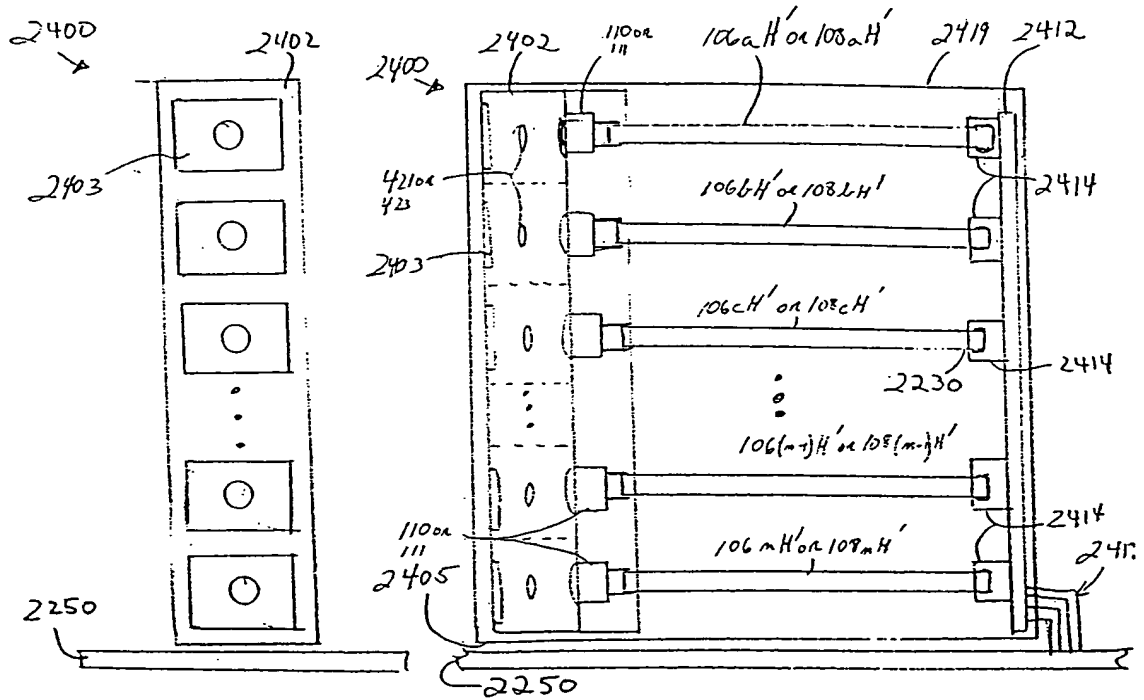
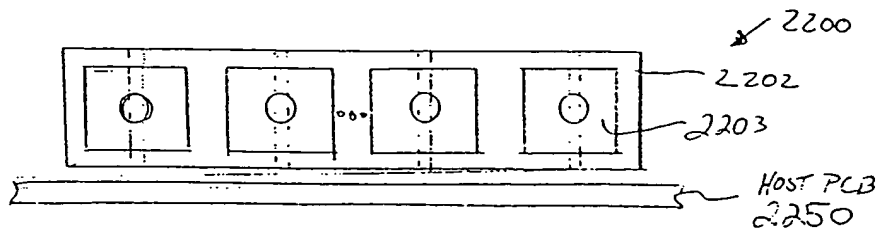
FIG. 20F

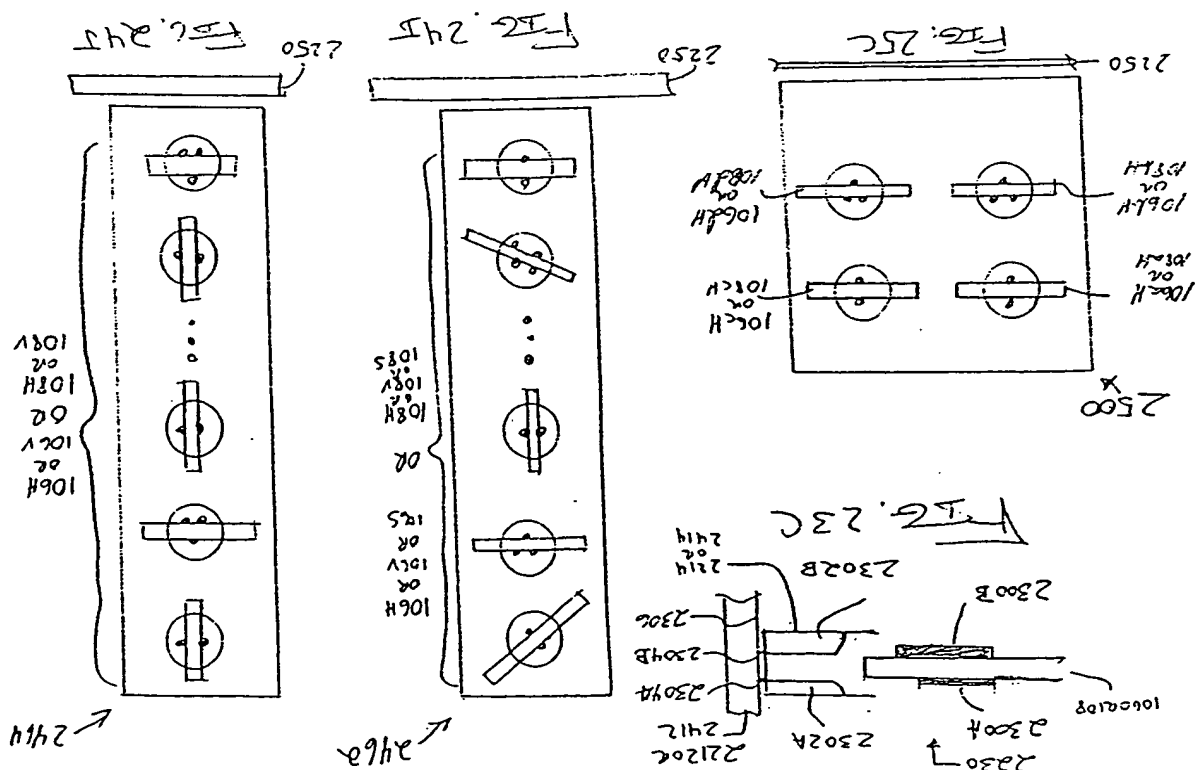
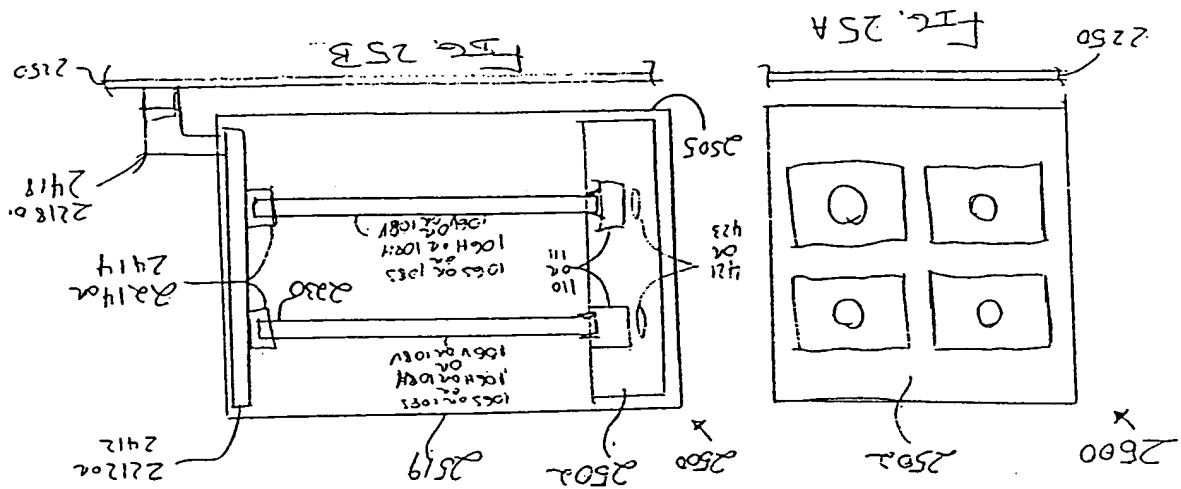


[illegible]

Hand-drawn schematic diagram of a multi-channel signal processing circuit. The diagram shows a vertical stack of four identical processing channels. Each channel consists of an input terminal (labeled 2200), a resistor (labeled 100 ohm), a variable gain control (represented by a potentiometer symbol), and an output terminal (labeled 2212). The output of each channel is connected to a common bus (labeled 2214) which is then connected to a multi-pin connector (labeled 2218). The connector is labeled "PINS OR ELECTRICAL CONNECTION". The diagram also shows a common ground connection (labeled 2214) for all channels. The input voltage for each channel is specified as 106mV or 108mV. The output voltage for each channel is specified as 106mV or 108mV. The diagram is labeled with various reference numerals: 2200, 100 ohm, 106mV or 108mV, 2212, 2214, 2218, and PINS OR ELECTRICAL CONNECTION.

FIG. 22B





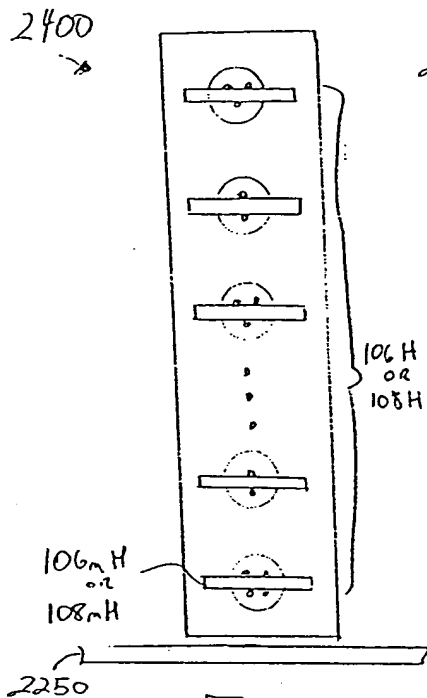


FIG. 24C

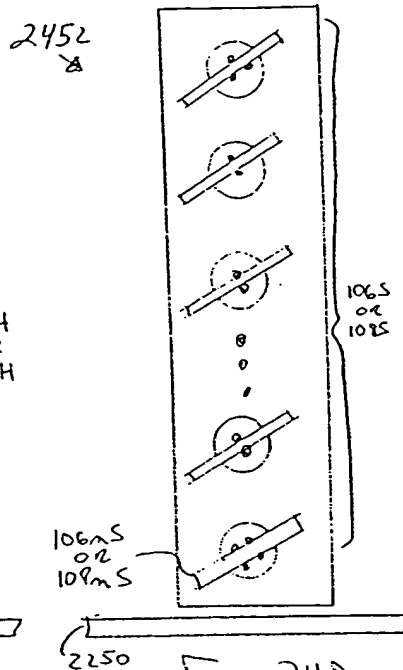


FIG. 24D

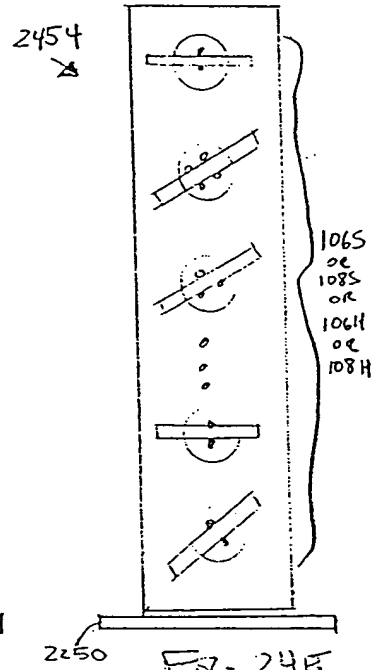


FIG. 24E

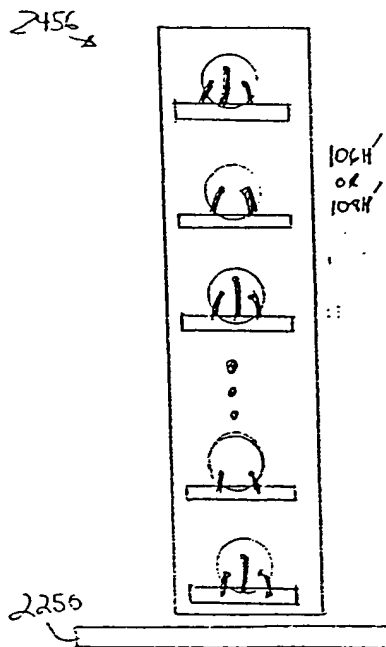


FIG. 24F

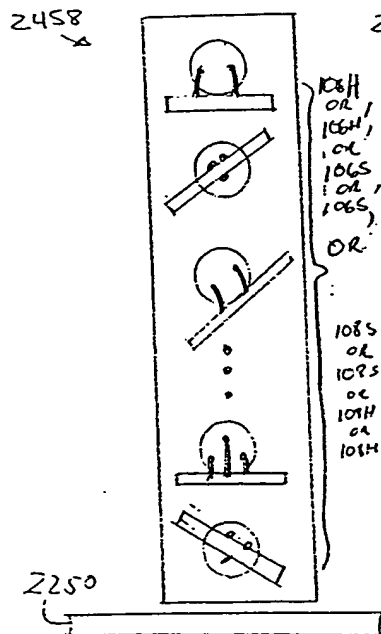


FIG. 24G

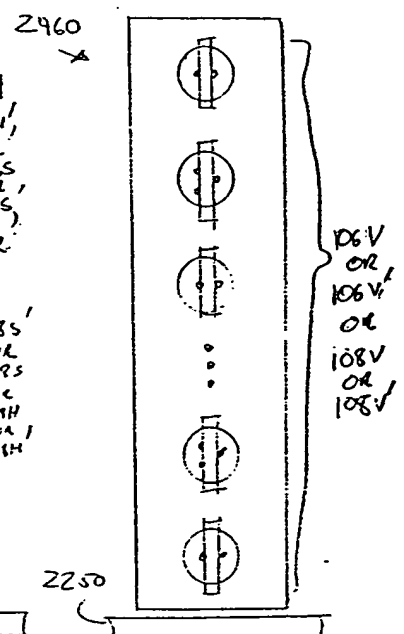


FIG. 24H

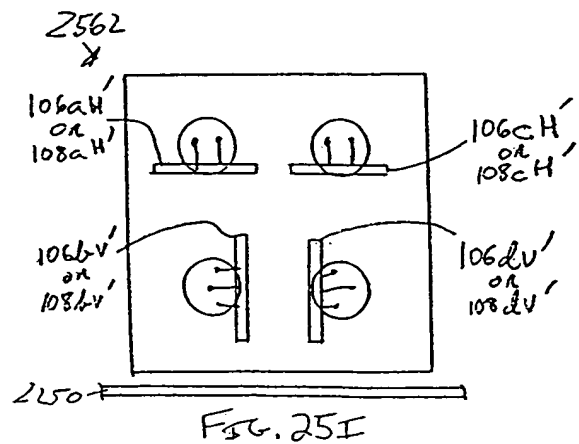
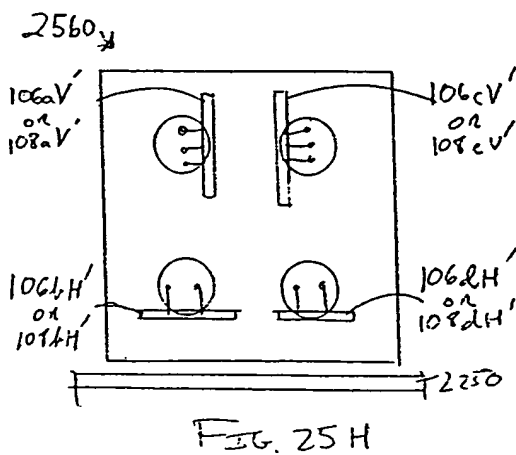
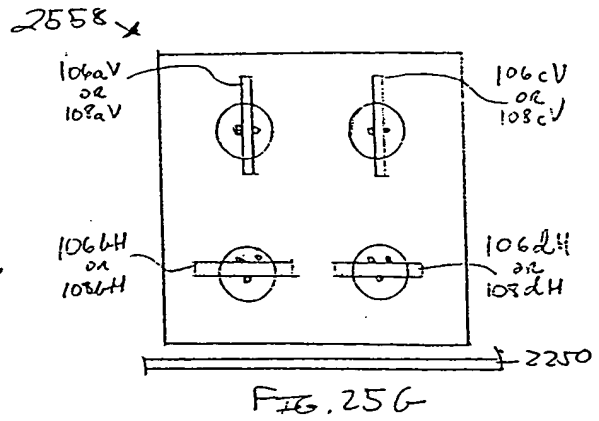
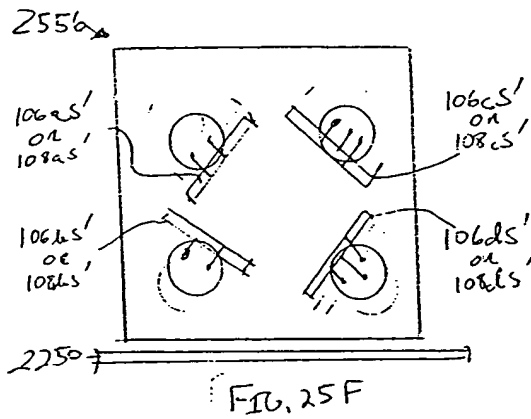
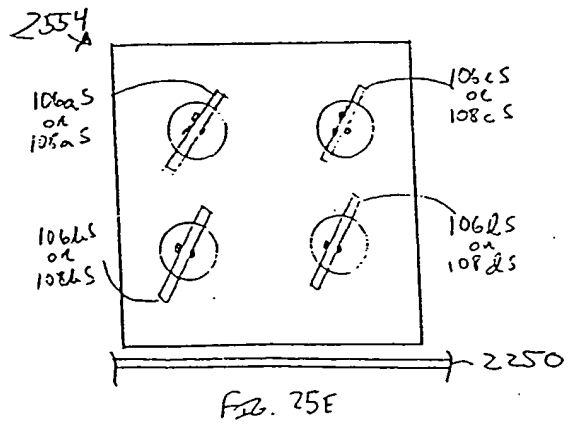
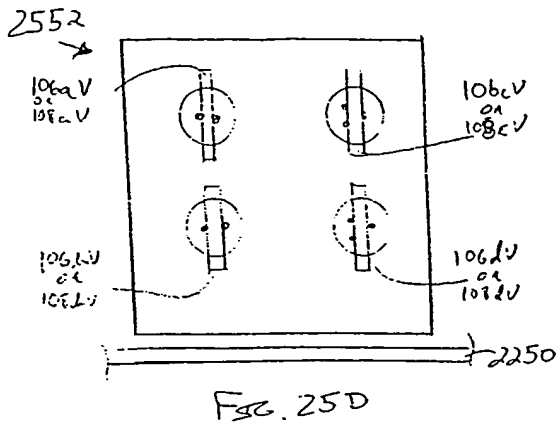


FIG. 26A

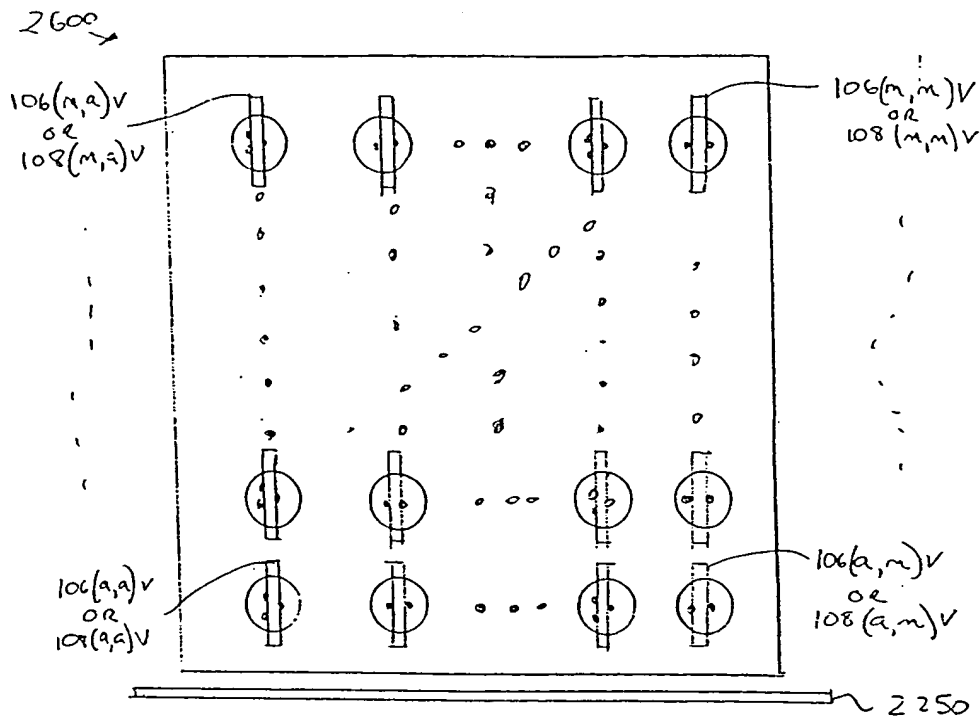


FIG. 26A

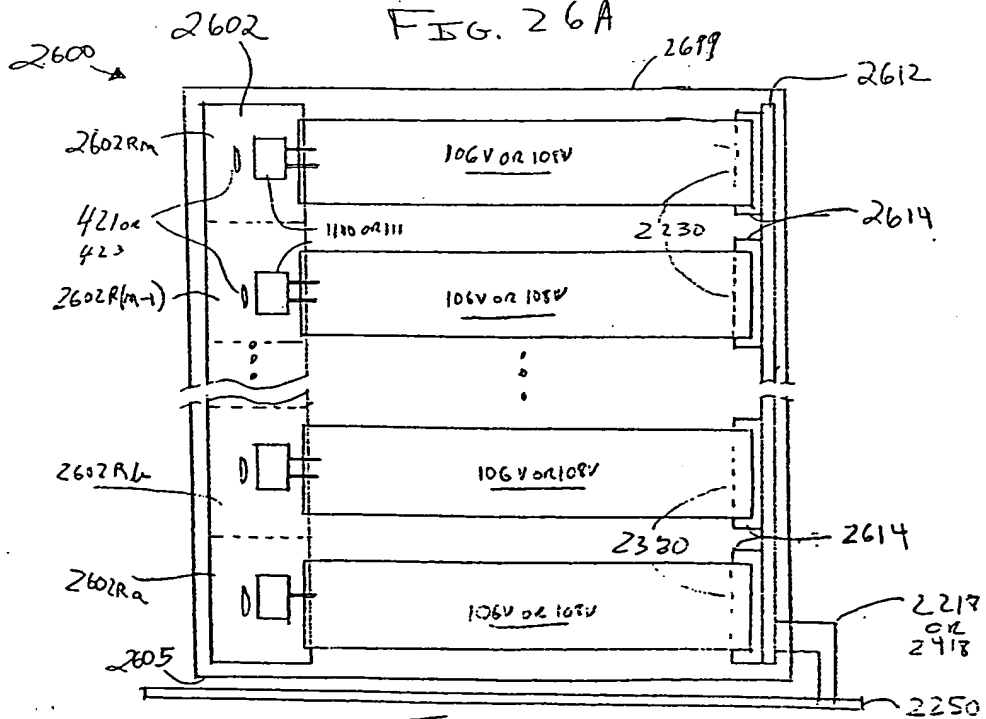


FIG. 26B

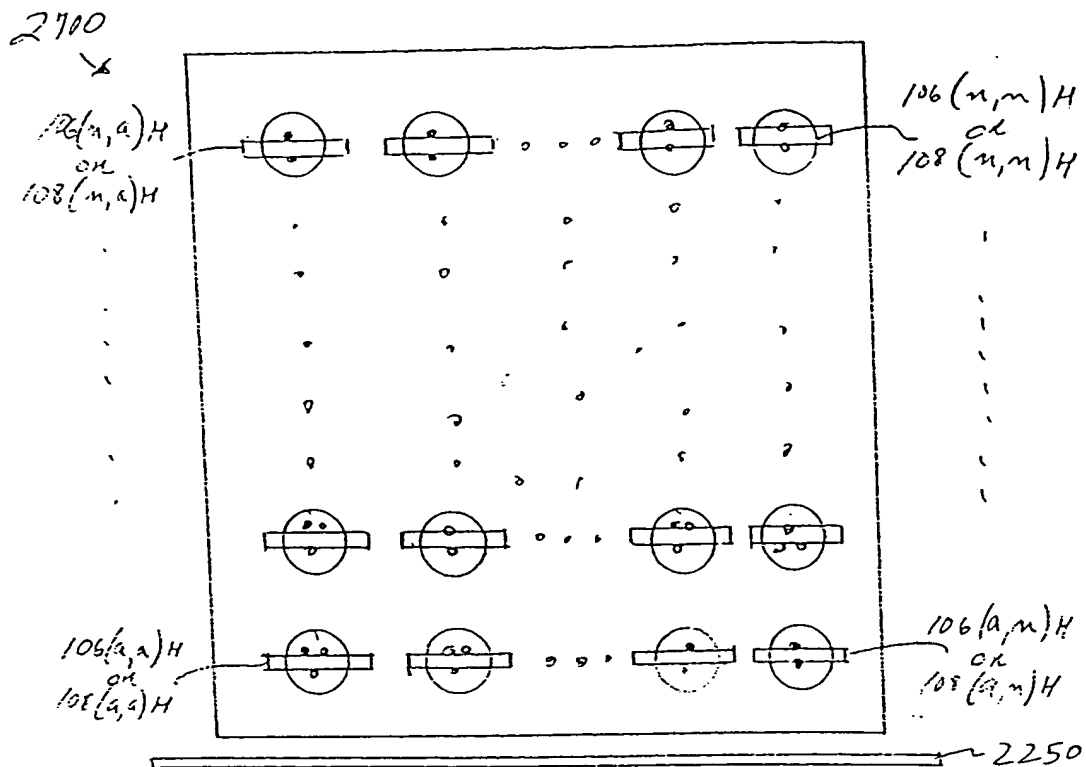


FIG. 27A

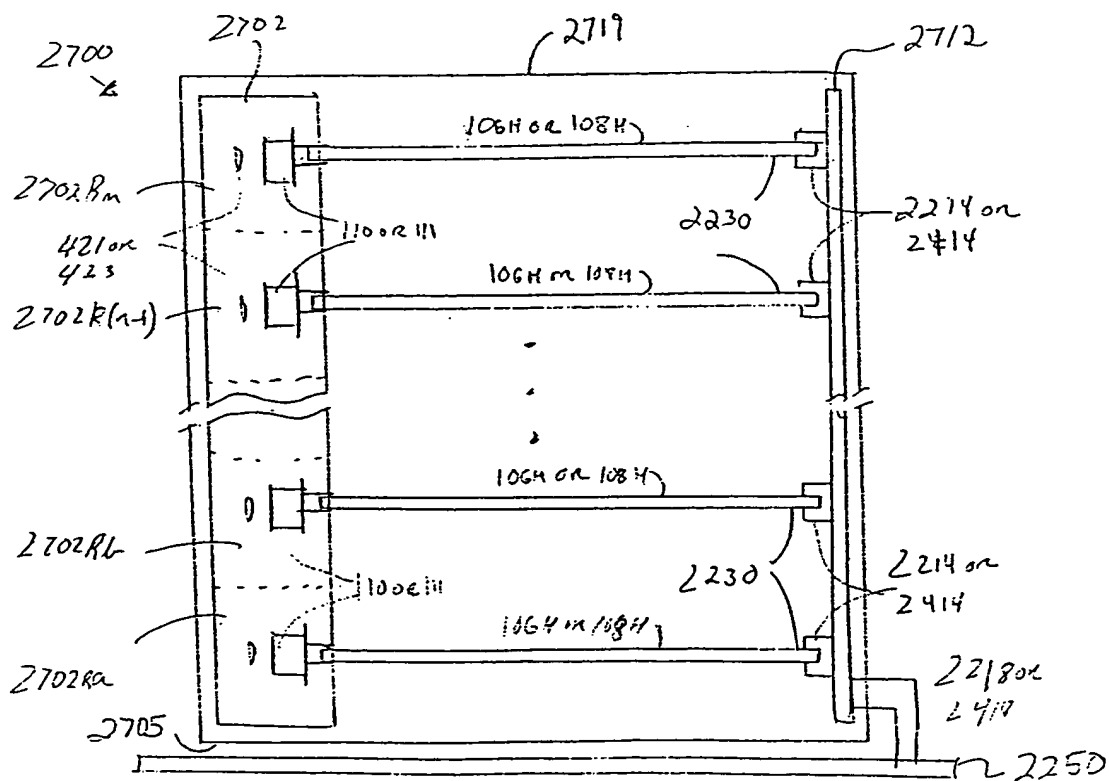


FIG. 27B

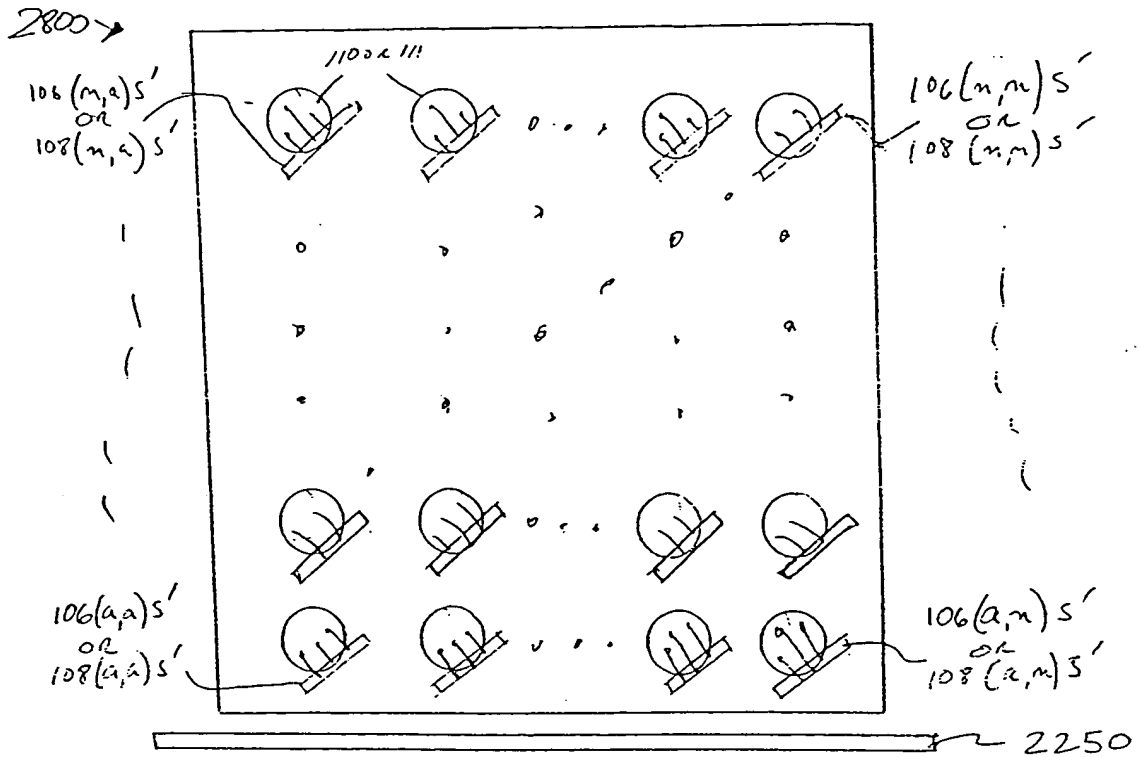


FIG. 28

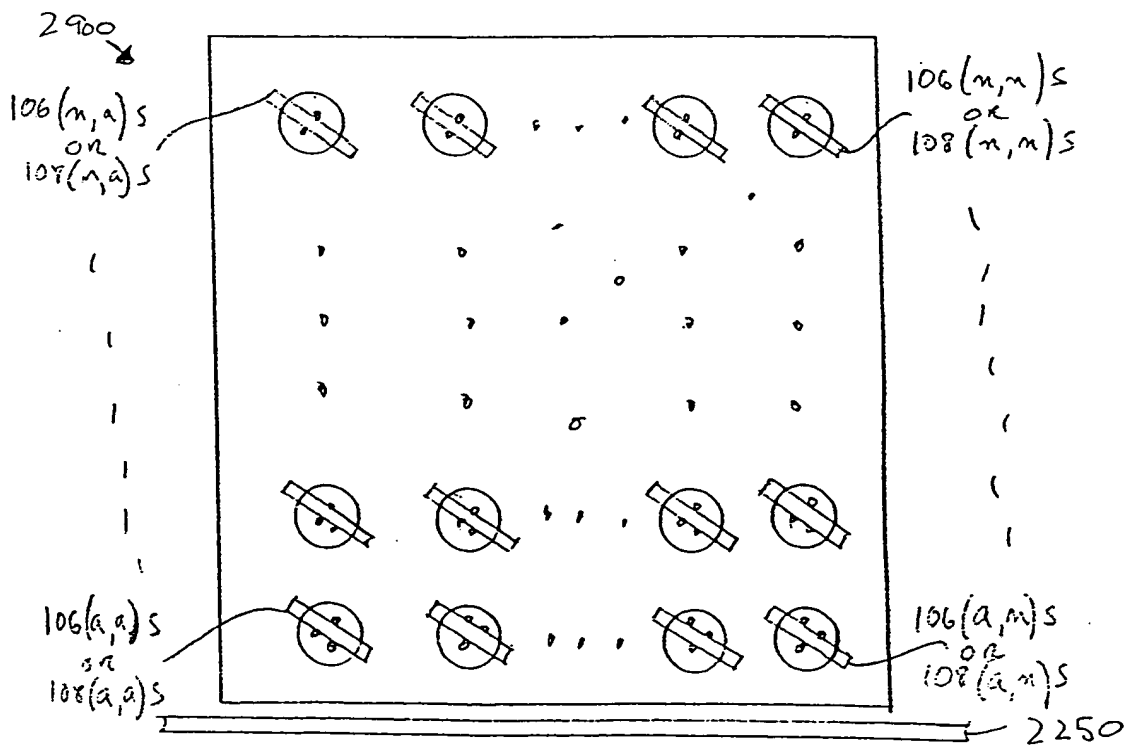


FIG. 29

TOPPED" BECEBQ

3000

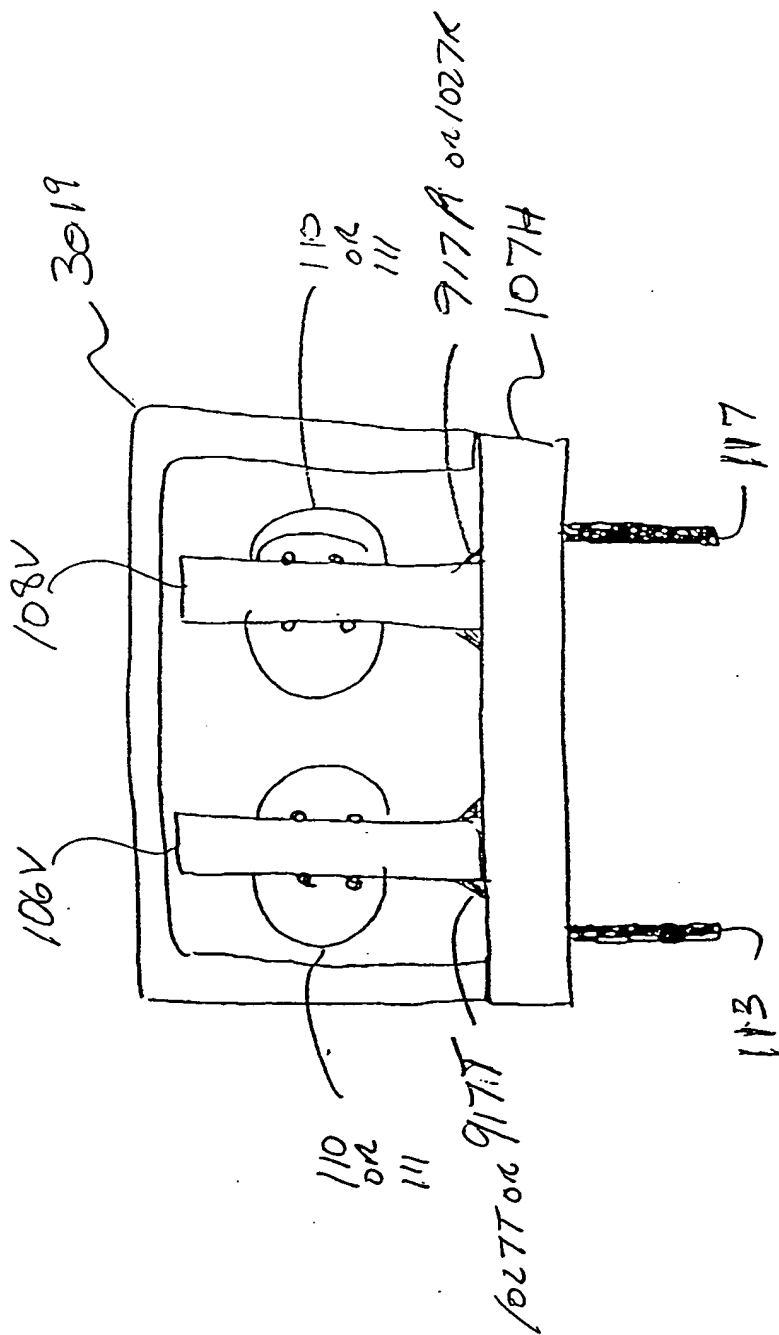


FIGURE 30

3/00

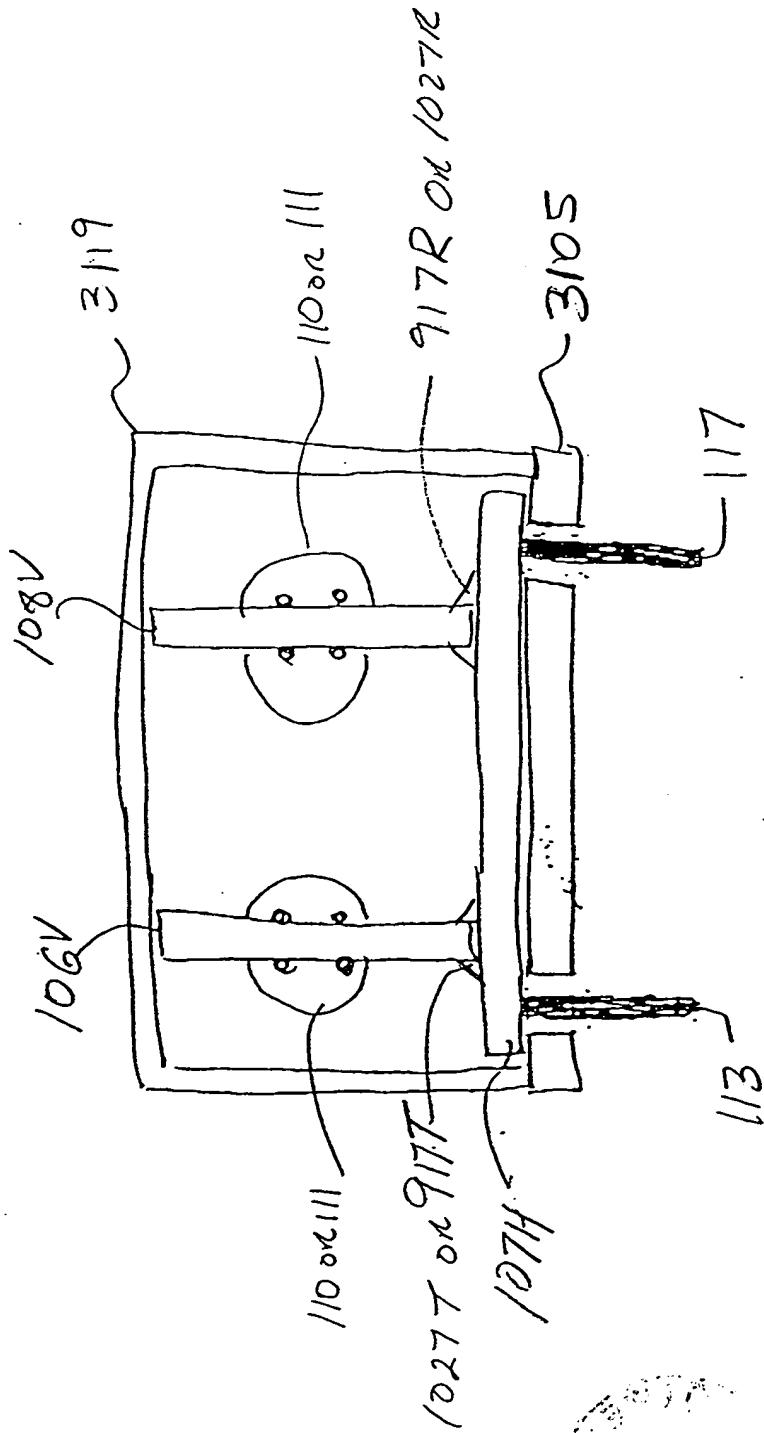


FIGURE 31

3200

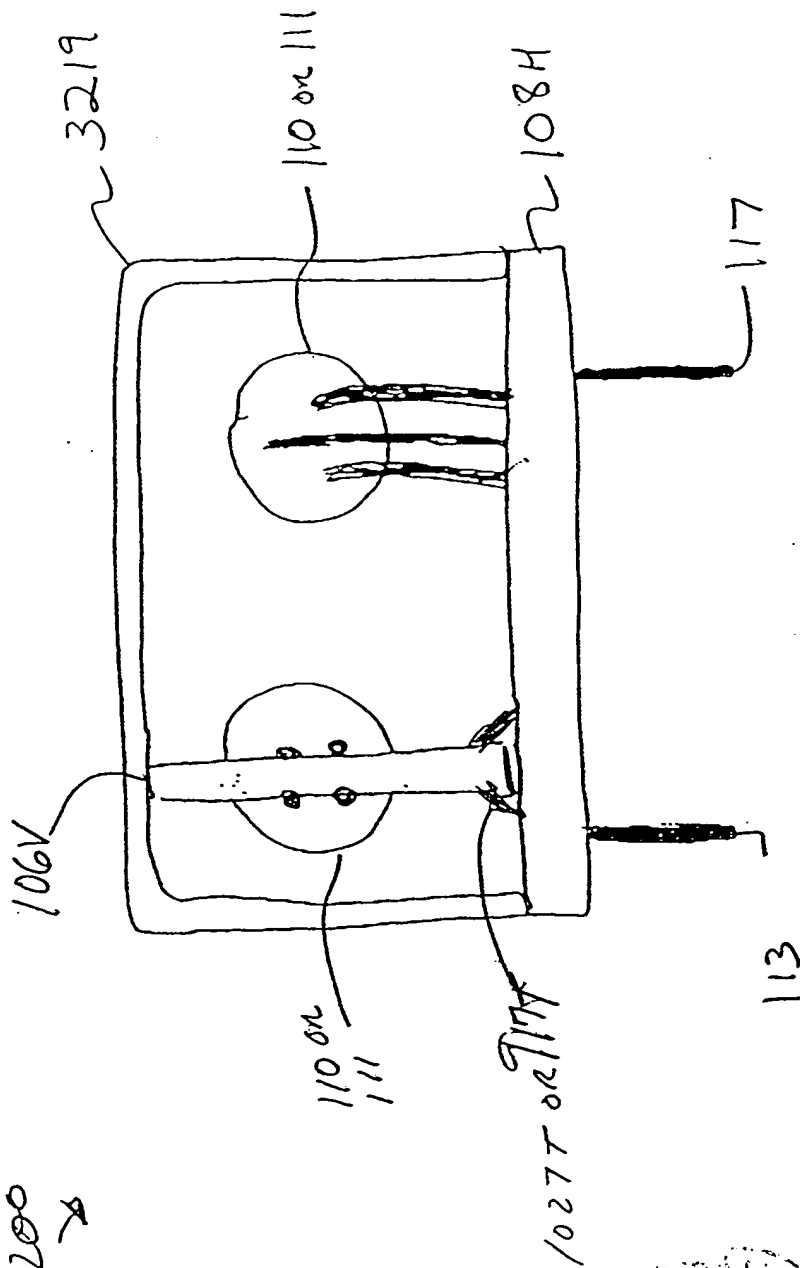


FIGURE 32:

TOP SECRET

3300

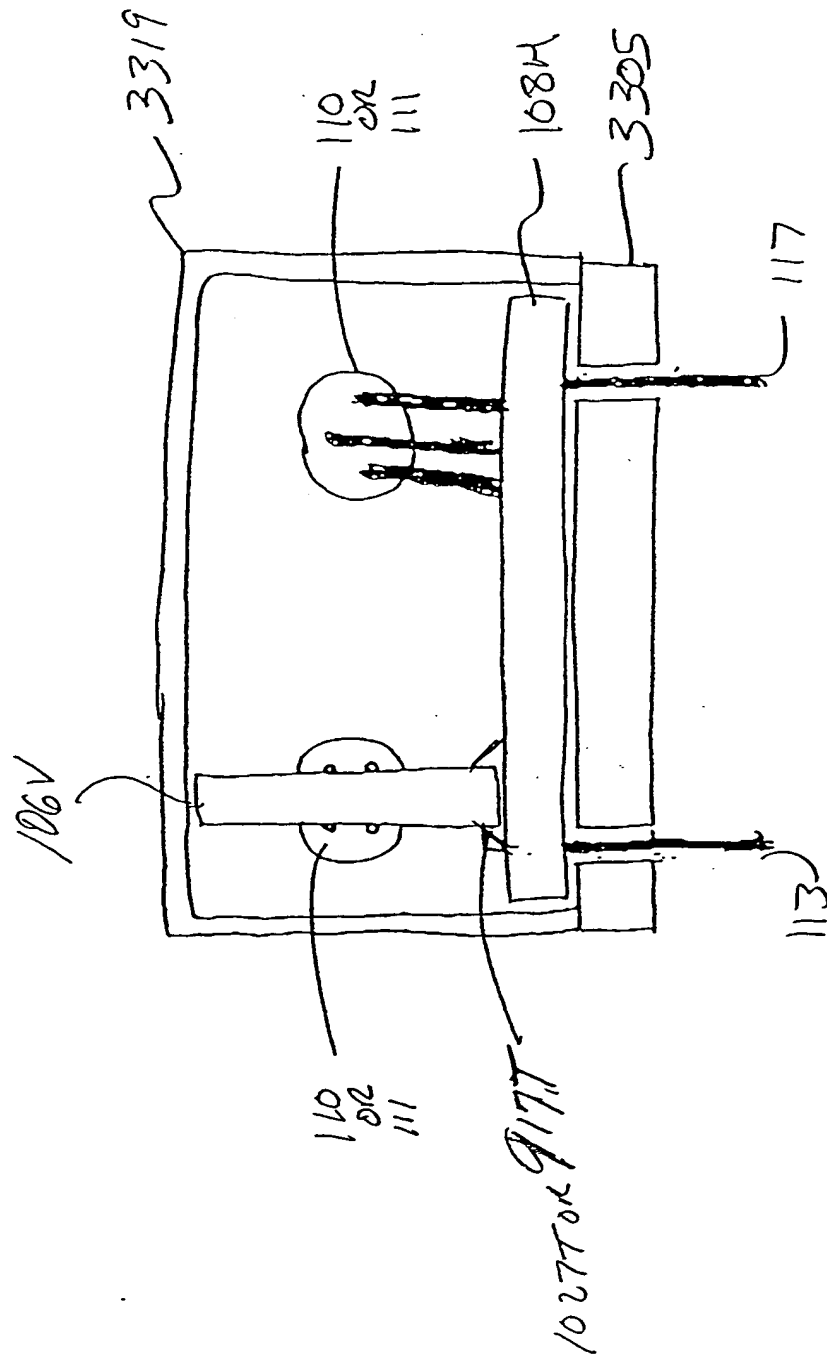


FIGURE 33: